A PULSED HIGH FREQUENCY PHASE DETECTOR WITH AN OUTPUT INTEGRATING CIRCUIT

William Richard Kurtz

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> "This research project represented a determined effort on the part of the student to arrive at the end result. Perseverance brought an otherwise average performance to the graduate level."

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ABSTRACT

The basic principles of phase detectors and pulse integrating circuits have been understood for many years. Most of the developmental work done on phase detectors has been concentrated on circuits designed to operate at audio or power frequencies. Pulse integrating circuits were not in demand until equipment involving the use of pulsed signals was constructed.

A critical investigation of three high frequency phase detectors is made in an effort to determine the operational limitations of each. The phase detectors studied operate at a frequency of 30 megacycles; the input signals to these detectors are pulses of energy at the carrier frequency. The duration of these input pulses is expected to be between 500 and 4000 pulses per second.

The effect on the operation of each circuit by an inequality in the amplitudes of the input signals is investigated. Effects of a deviation from the operating frequency of 30 megacycles are studied. A study is made of the minimum pulse width of the input signals which can be used and yet furnish reliable output signals. One requirement which must be met by each circuit is that there must be no output when one of the two input signals is zero.

When there is a constant rate of change of phase between the two input signals to a phase detector, the

amplitude of the output pulse will be varying at a cyclic rate. A pulse-integrating circuit is connected to the output of the phase detector to integrate the information denoted by the amplitude of the output pulses. The output from the pulse-integrating circuit is used to determine the envelope frequency of the phase detector output pulses.

The output of a 30 megacycle signal generator is pulse-modulated, and the output sent to a phase detector through two paths. Located in one path is a circuit capable of introducing an amount of phase shift which can be varied from 0 to 360 degrees. The operating characteristics of the three phase detectors are studied for wide variations in the amplitude, duration, and carrier frequency of the input pulses. Each phase detector is also tested using CW input signals.

For testing the pulse-integrating circuit, a constant rate of change of phase between the two inputs to a phase detector is introduced. With the amplitude of the output pulse from a phase detector varying at some definite frequency, the output of the pulse-integrating circuit is studied for different pulse repetition frequencies and different pulse widths.

The results of the tests made on the phase detectors indicated that the simplest circuit operated best, while the most complex circuit introduced undesirable distortion. The diode pulse-integrating circuit tested does not operate

satisfactorily if the pulse repetition frequency is less than 500 pulses per second or if the input pulse is less than one microsecond in duration.

A PULSED HIGH FREQUENCY PHASE DETECTOR
WITH AN OUTPUT INTEGRATING CIRCUIT

by

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CHAPTER I

INTRODUCTION AND STATEMENT OF THE PROBLEM

The basic principles of phase detectors and pulse integrating circuits have been understood for many years. Most of the developmental work done on phase detectors has been concentrated on circuits designed to operate at audio or power frequencies. Pulse integrating circuits were not in demand until equipment involving the use of pulsed signals was constructed.

The increasing use of microwaves for radar and communications has aroused interest in high frequency phase detectors. A need for phase comparison of two signals at the intermediate frequencies used in the microwave equipment has arisen, and the development of units to perform this function has been initiated. A critical investigation of the operating characteristics of three high frequency phase detectors will be made in an effort to determine the operational limitations of each.

The phase detectors to be studied operate at a frequency of 30 megacycles; the input signals to the phase detectors are to be pulses of energy at the carrier frequency. The duration of these input pulses is expected to be between 0.5 and 10 microseconds, and the pulse repetition frequency is to be between 500 and 4000 pulses per second.

A phase detector develops an output voltage proportional to the relative phase angle existing between the two input signals. One of the stipulated requirements to be met by each phase detector is that there must be no output when one of the two input signals is zero. The effect on the operation of each circuit by an inequality in the amplitudes of the input signals will be investigated. Another factor to be considered is the effect on circuit performance produced by a deviation from the operating frequency of 30 megacycles.

The need has arisen for definite information regarding the minimum pulse width of the input signals which can be used and yet furnish reliable output signals. A study of the minimum pulse width involves a determination of the number of cycles of the carrier frequency in the input signal which must be compared in the phase detector to provide an output signal whose amplitude varies with the phase angle existing between the two input signals. The effects of changing the pulse repetition frequency will also be investigated.

With the advent of pulse-time-modulation communication systems and radar installations, circuits have been designed which integrate pulses of varying amplitude occurring at periodic intervals. The majority of these circuits have been designed to handle input pulses of one polarity only, usually positive. To integrate the output pulses from a

phase detector, a circuit which is capable of accepting input pulses of both polarities must be used. Of major interest in the investigation of the output integrating circuit are the effects of the pulse repetition frequency, pulse width, and pulse amplitude upon the integrated output.

A block diagram of the equipment used to test the 30 megacycle phase detectors and the pulse-integrating circuit is shown in Fig. 1-1. Some of the equipment shown in the diagram is available commercially; the remainder was constructed in the laboratory.

The manufactured units of the block diagram are listed as follows:

Model 200 Hewlett Packard Audio Oscillator (used to determine the pulse repetition frequency)

2 General Radio Co. 869-A Pulsers (one negative pulse output and one positive pulse output)

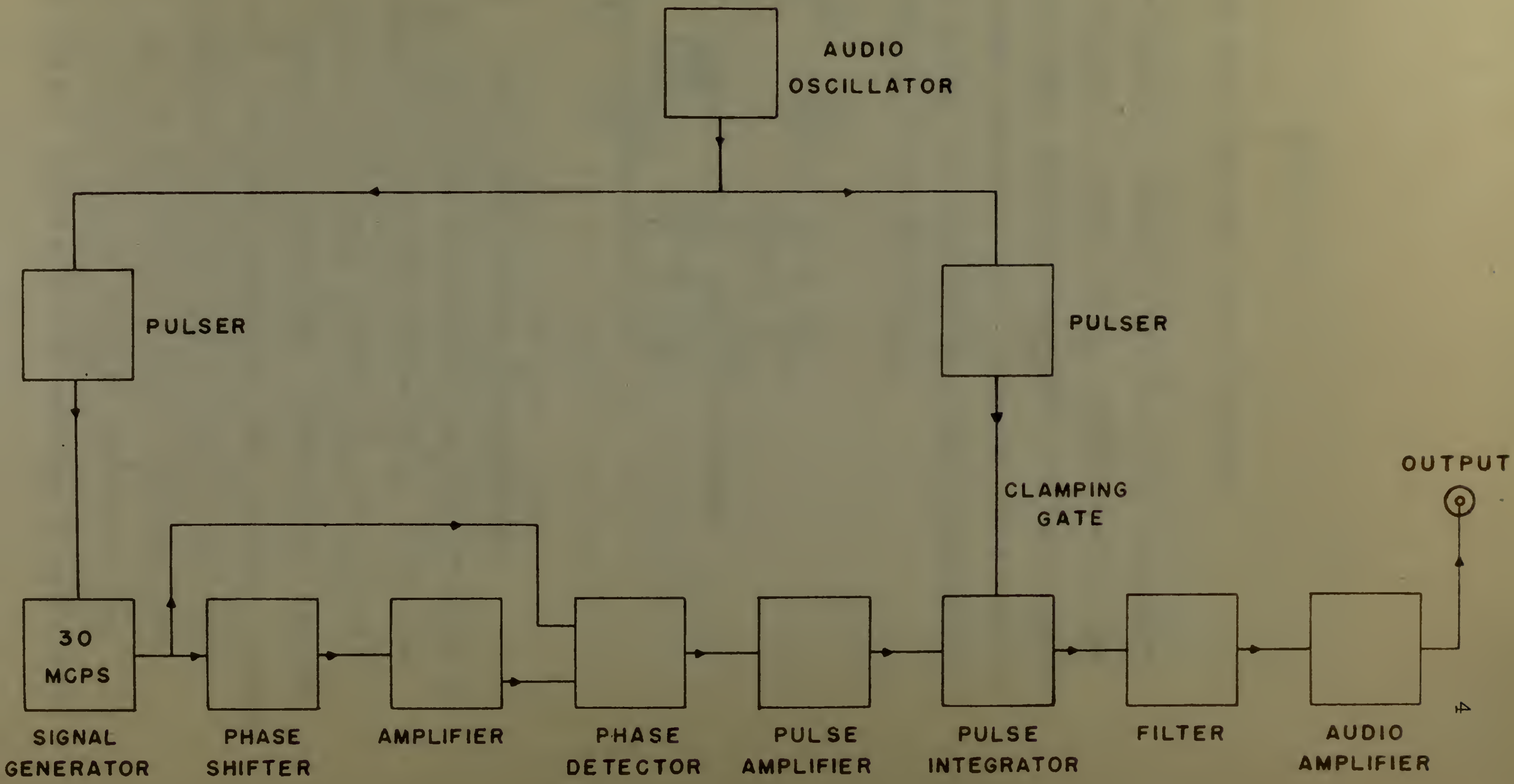
General Radio Co. Signal Generator 805-AS1 (a special model capable of being pulse modulated)

Model 300 Ballantine Electronic Voltmeter (used as an audio amplifier)

The 30 megacycle amplifier shown in the block diagram was an AN/APS-10 I.F. amplifier strip with the detector stage removed. The remainder of the units are described in the succeeding chapters.

FIG. 1-1

BLOCK DIAGRAM OF EQUIPMENT USED TO TEST PHASE DETECTORS AND PULSE INTEGRATOR



CHAPTER II

A STUDY OF 30 MEGACYCLE PHASE DETECTORS

A phase detector, sometimes called a phase sensitive rectifier, develops an output voltage proportional to the relative phase angle existing between the two input signals. The basic circuit diagram of a low frequency phase detector is presented in Fig. 2-1 (a), and the circuit operation is explained with the aid of the diagram.

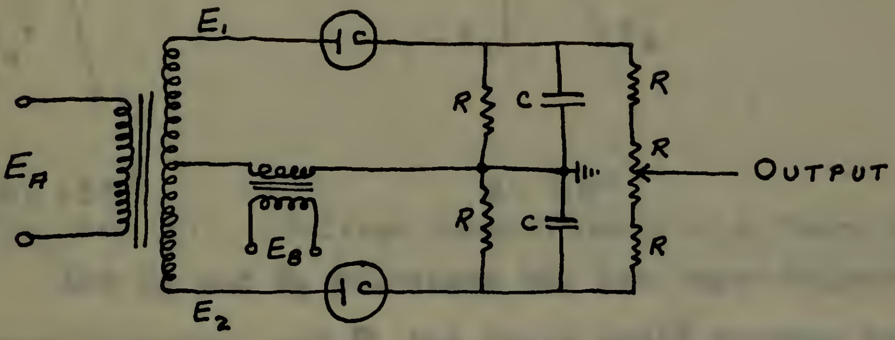


Fig. 2-1 (a)   Basic Low-Frequency Phase Detector

A more or less standard procedure has been developed to obtain the desired output at low frequencies. One of the two input signals to the phase detector, E_a, is applied to the primary winding of a transformer. The voltages induced by E_a appearing at the end terminals of the secondary winding are of equal magnitude but 180° out of phase. The second input signal, E_b, is introduced as shown, combining with the secondary voltages induced by E_a to produce two new voltages, E_1 and E_2. These voltages represent a vector sum

and vector difference of the two input signals. This can be illustrated with the aid of the vector diagrams shown in Fig. 2-1 (b).

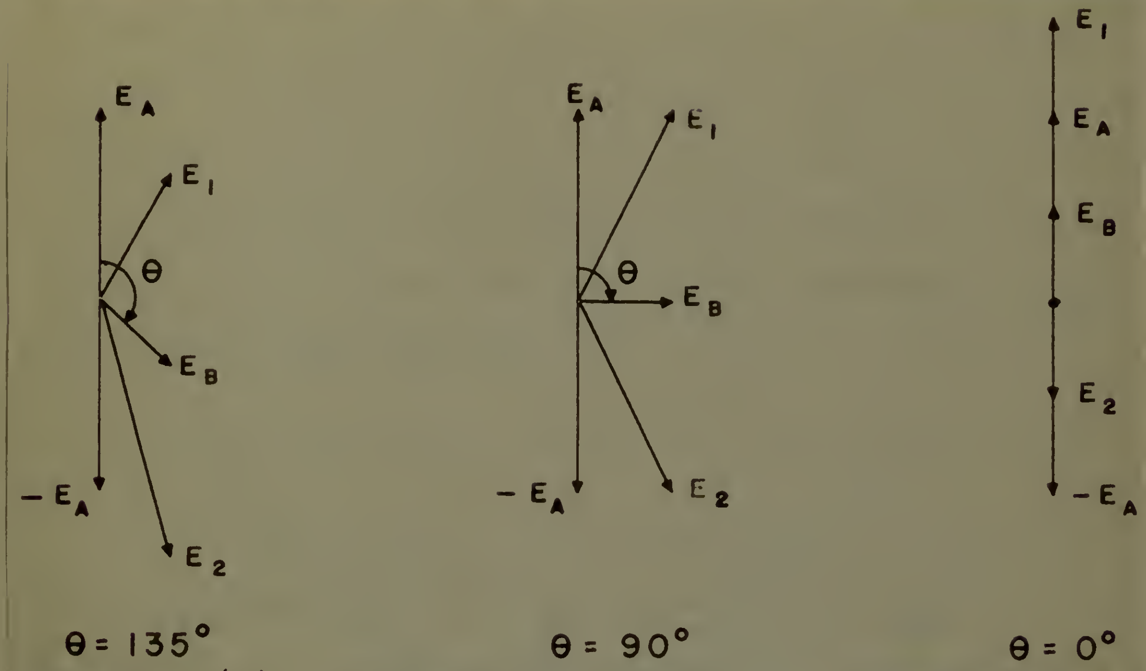


Fig. 2-1 (b) Voltage Relationship in a Phase Detector

Let E_a and E_b represent the two input signals to the phase detector, and θ the phase angle between the inputs. Signal E_a is split into two equal vectors, 180° out of phase, E_a and $-E_a$. Signal E_b is added vectorially to E_a and $-E_a$: the vector sum $E_b + E_a$ is represented by E_1, and the vector difference $E_b - E_a$ represented by E_2. Signals E_1 and E_2 are rectified, filtered, and the two resultant d-c voltages are added differentially at the center tap of a resistance mixer. The final d-c output signal is essentially the difference of the two rectified signals. Assuming equal detector efficiences, if E_1 is greater in magnitude than E_2, the output signal is positive; if E_2 is the

larger, the output signal is negative.

A study of the three diagrams in Fig. 2-1 (b) reveals that the output from the detector will vary approximately as the cosine function of θ. When $\theta = 0^\circ$, $|E_1| - |E_2|$ is a positive maximum; when $\theta = 180^\circ$, $|E_1| - |E_2|$ is a negative maximum, and the output will be zero when $\theta = 90^\circ$ or 270°. A simple sketch of the expected phase detector output as a function of phase difference between the input signals is shown in Fig. 2-1 (c).

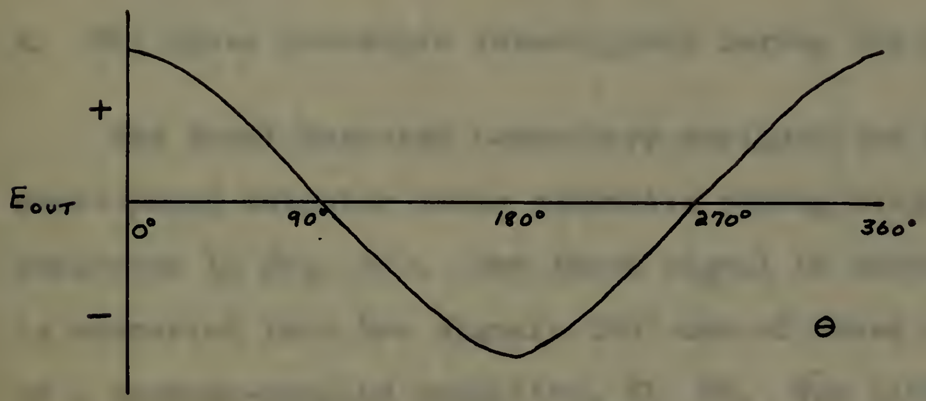


Fig. 2-1(c) Output as a Function of Phase Difference

Once the principles of operation have been established, it becomes a matter of circuit technique to create a practical phase detector.

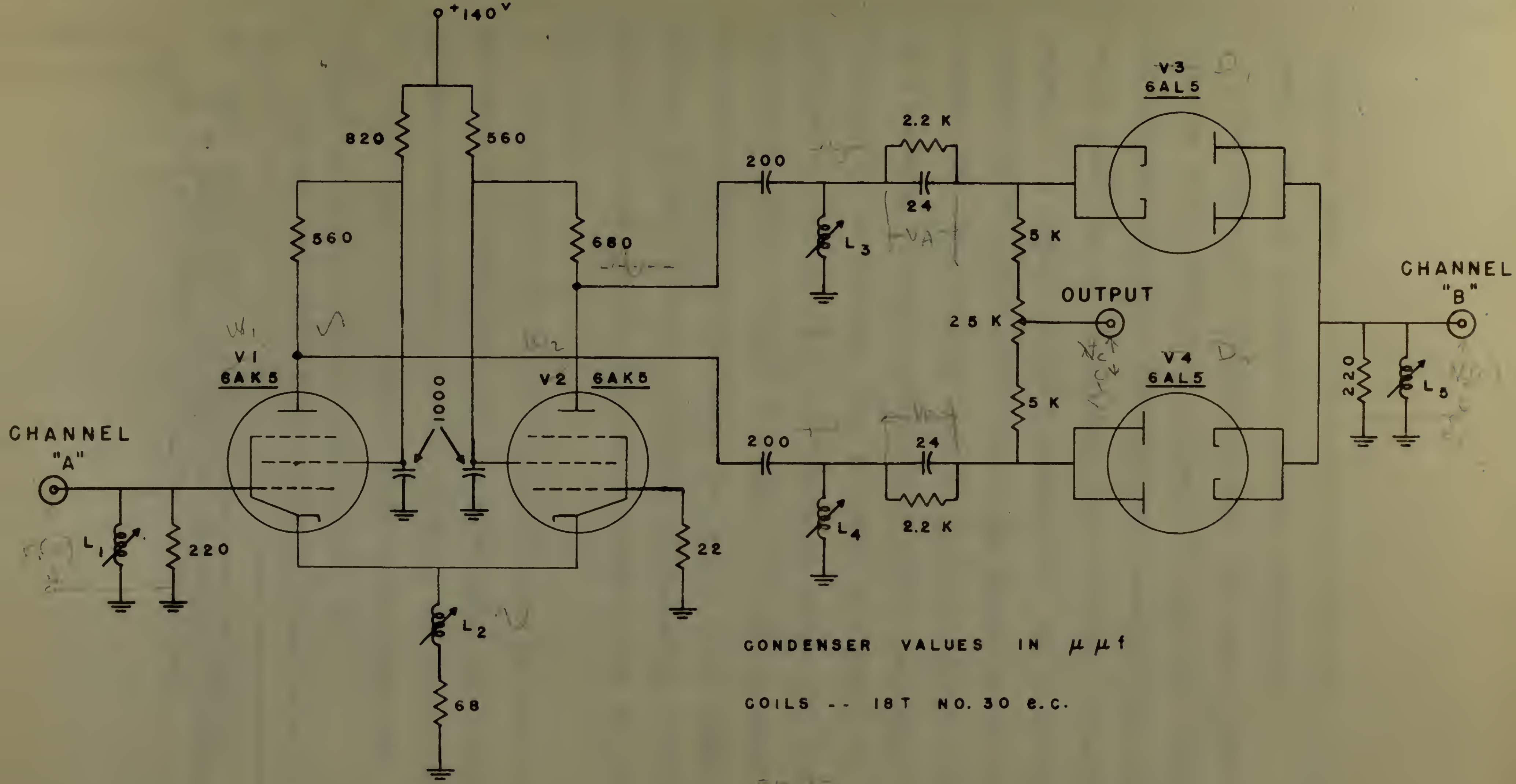
The early development of phase detectors has been concentrated on circuits to be used at audio or power frequencies. Low frequency phase detectors are frequently used in servomechanism applications. However, there is considerable interest in phase detectors which will operate satisfactorily at frequencies of many megacycles.

This chapter will be devoted to a study of three different phase detectors which operate at 30 megacycles.

At low frequencies the problem of splitting one input signal into equal and opposite vectors has been solved by using transformers. Such equipment is not feasible when the frequency of the input signal is 30 megacycles; the phase splitting is performed in amplifier stages. A description of the operation of a 30 megacycle phase detector will explain the preceding statement more fully.

A. The Phase Detectors Investigated During the Research.

The Naval Research Laboratory designed the 30 megacycle phase detector whose schematic wiring diagram is presented in Fig. 2-2. The input signal to channel "A is converted into two signals 180° out of phase by means of a cathode-coupled amplifier, V1 V2. The plate load resistors of these miniature pentodes are adjusted to provide equal signal voltages at the plates of V1 and V2. These two equal and out-of-phase voltages are then fed into two diodes connected back-to-back. The other side of each diode is supplied with the second input signal. Thus the output voltage developed by each diode is dependent upon the phasing and amplitude of the plate and cathode signals. The diode detector loads consist of 2200 ohms in parallel with 24μμf. In operation, the output of each diode is added differentially at the center-tap of a



CONDENSER VALUES IN $\mu\mu f$

COILS -- 18T NO. 30 e.c.

FIG. 2-2

NRL PHASE DETECTOR

resistance mixer, with the center-tap adjustable to compensate for any unbalance in circuit parameters.

The schematic wiring diagram of the second phase detector being studied is presented in Fig. 2-3. This differential amplifier phase detector accomplishes the vector addition of two voltages in a somewhat different manner.[1] A cathode-coupled amplifier V1 V2 is used to accomplish the phase splitting of the signal applied to channel "A". The cathode load for this amplifier consists of a pentode, with the second input signal introduced on the grid of the pentode, V3. A signal in channel "A" will produce two voltages 180° out of phase across the load resistors, while a signal in channel "B" will produce two in-phase voltages across these resistors. With signals applied to both channels, voltages representing a vector sum and a vector difference are produced across the 1K resistors.

The voltages produced at the plates of V1 and V2 are fed into two diodes connected back-to-back. The output of each diode is added differentially at the center-tap of a resistance mixer, and the final output taken off through a cathode-follower output stage, V6.

The NRL and differential amplifier phase detectors

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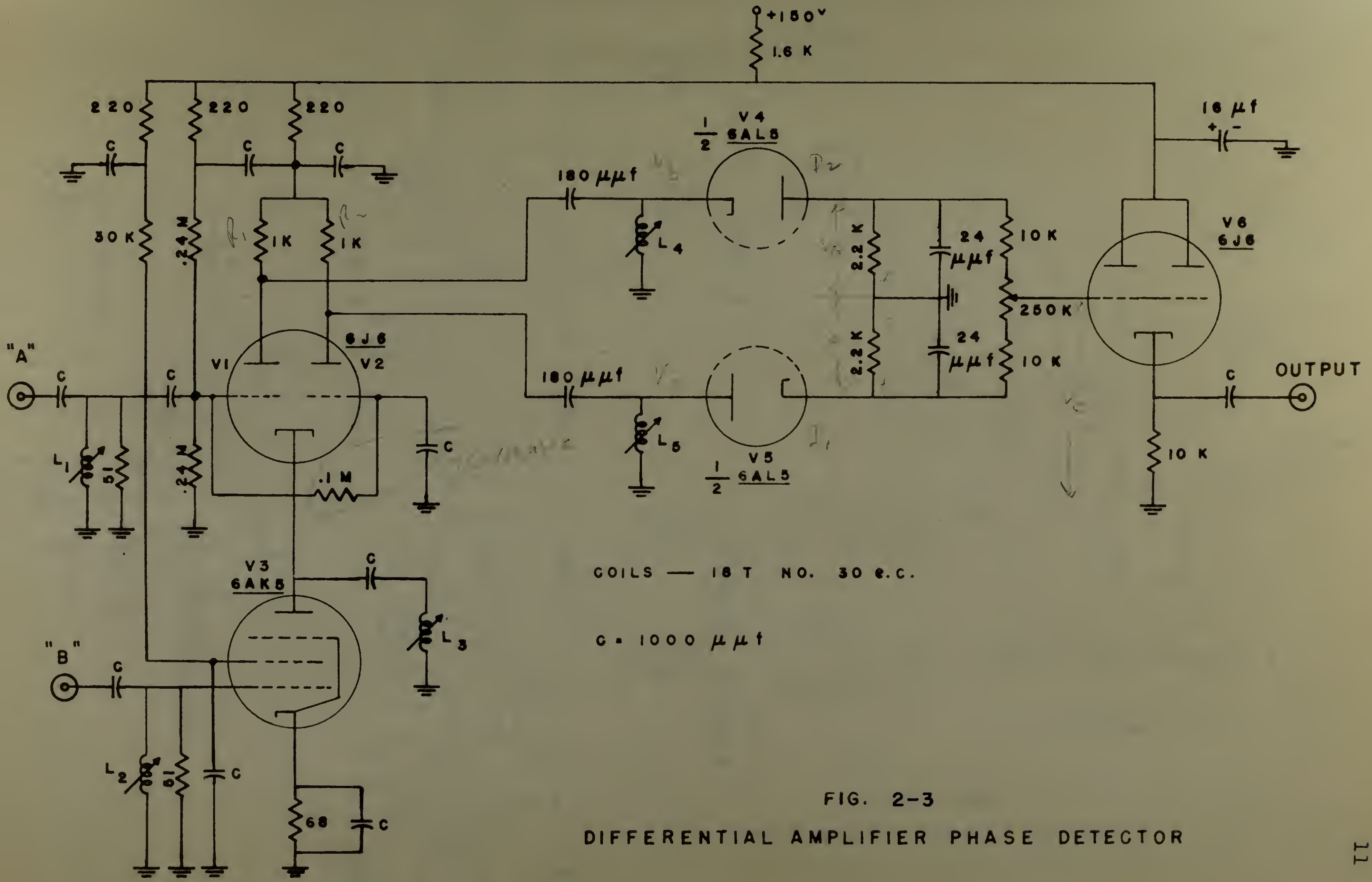
1. This 30 megacycle phase detector was designed by W. B. Renhult of the Research Laboratory of Electronics at the Massachusetts Institute of Technology.

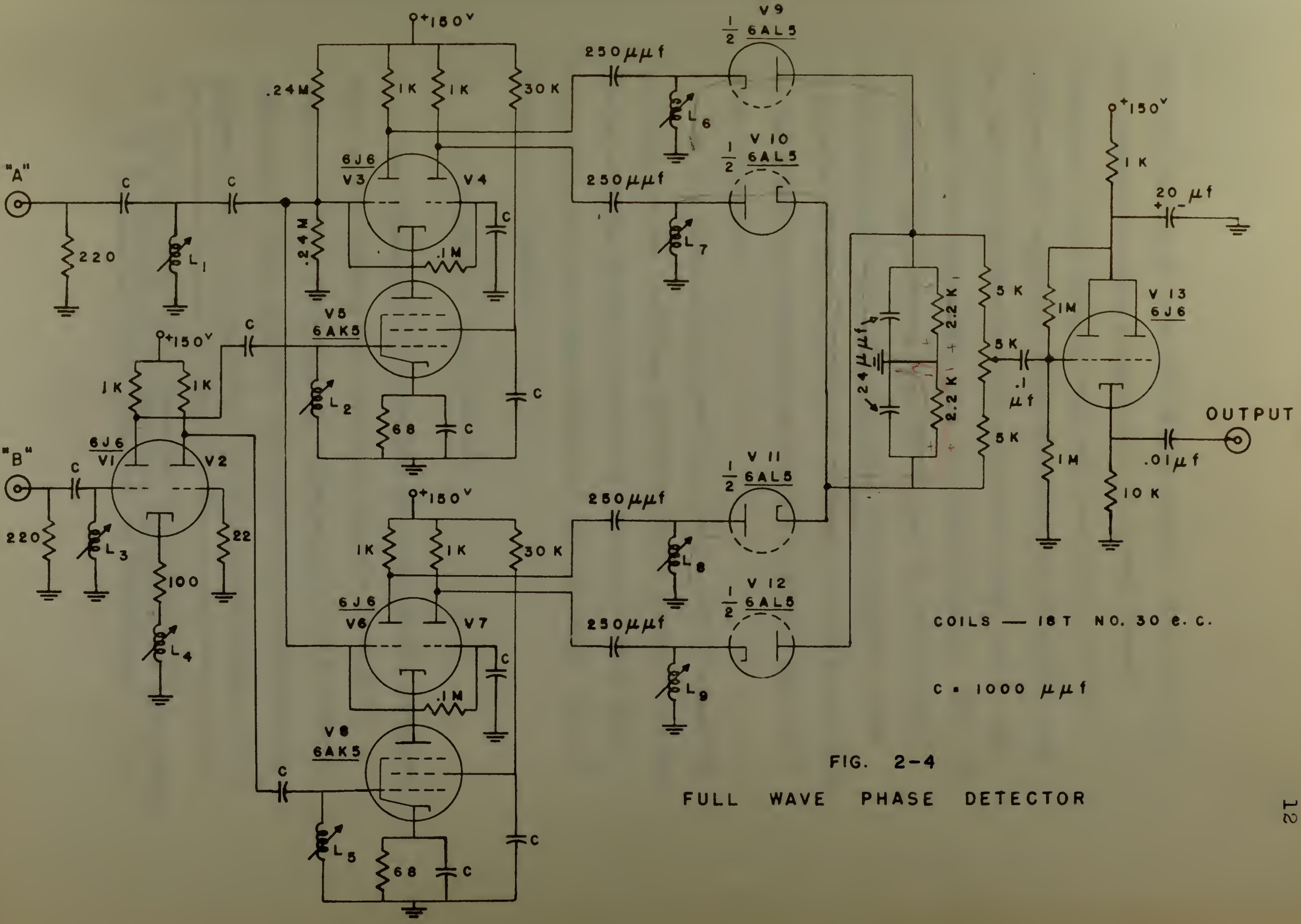


COILS — 18 T NO. 30 e.c.

C = 1000 μμf

FIG. 2-3

DIFFERENTIAL AMPLIFIER PHASE DETECTOR



COILS — 18T NO. 30 e. c.

C = 1000 μμf

FIG. 2-4

FULL WAVE PHASE DETECTOR

contain only half-wave rectifying stages. Fig. 2-4 is the schematic wiring diagram of a full-wave phase detector.[2] This circuit consists essentially of two differential amplifier phase detectors in parallel, with the addition of another phase splitter which splits the channel "B" input signal into two equal vectors, 180° out of phase. The outputs from V3 V4 and V6 V7 are fed into two pairs of diodes connected back-to-back. From that point on the operation is identical to that described in the preceding paragraph on the differential amplifier phase detector.

In all three phase detectors, small chokes are used to resonate the input capacitances to the phase-splitting stages and the diodes. Miniature tubes have been used throughout and the construction of the detectors made as compact as possible.

B. A 30 Megacycle Phase Shifter

Some means must be provided for varying the relative phase angle between the two input signals to a phase detector. At a frequency of 30 megacycles the problem of obtaining a phase shifter which operates satisfactorily becomes acute. A schematic wiring diagram of the circuit

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[2] The full wave phase detector was designed by [illegible]. B. Renhult of the Research Laboratory of Electronics at the Massachusetts Institute of Technology.

used is presented in Fig. 2-5.[3] A brief explanation of the phase shifter's operation is necessary for clarity.

Located in the grid circuits of V1 and V3 are RC phase-shift networks designed to produce voltages which are in quadrature at the grids of these stages when the frequency of the input signal is 30 megacycles. Two cathode-coupled amplifiers split these signals into four equal voltages, separated in phase by 90 electrical degrees. The four signals are applied through isolating cathode followers to the plates of a Western Electric Phase Shift Capacitor. As the shaft carrying an eccentric dielectric plate is rotated, the output will be of constant amplitude, with the phase shift varying smoothly from zero to 360 electrical degrees. Attached to the shaft carrying the dielectric is a dial graduated from 0 to 360 degrees, to be read against a fixed pointer.

If two signals of the same frequency and of equal amplitudes are applied to the horizontal and vertical deflecting plates of an oscilloscope, the waveform appearing on the cathode ray tube will be either a circle, an ellipse of some shape, or a straight line, depending upon the phase relationship between the two input signals. When the amount of phase difference between the two

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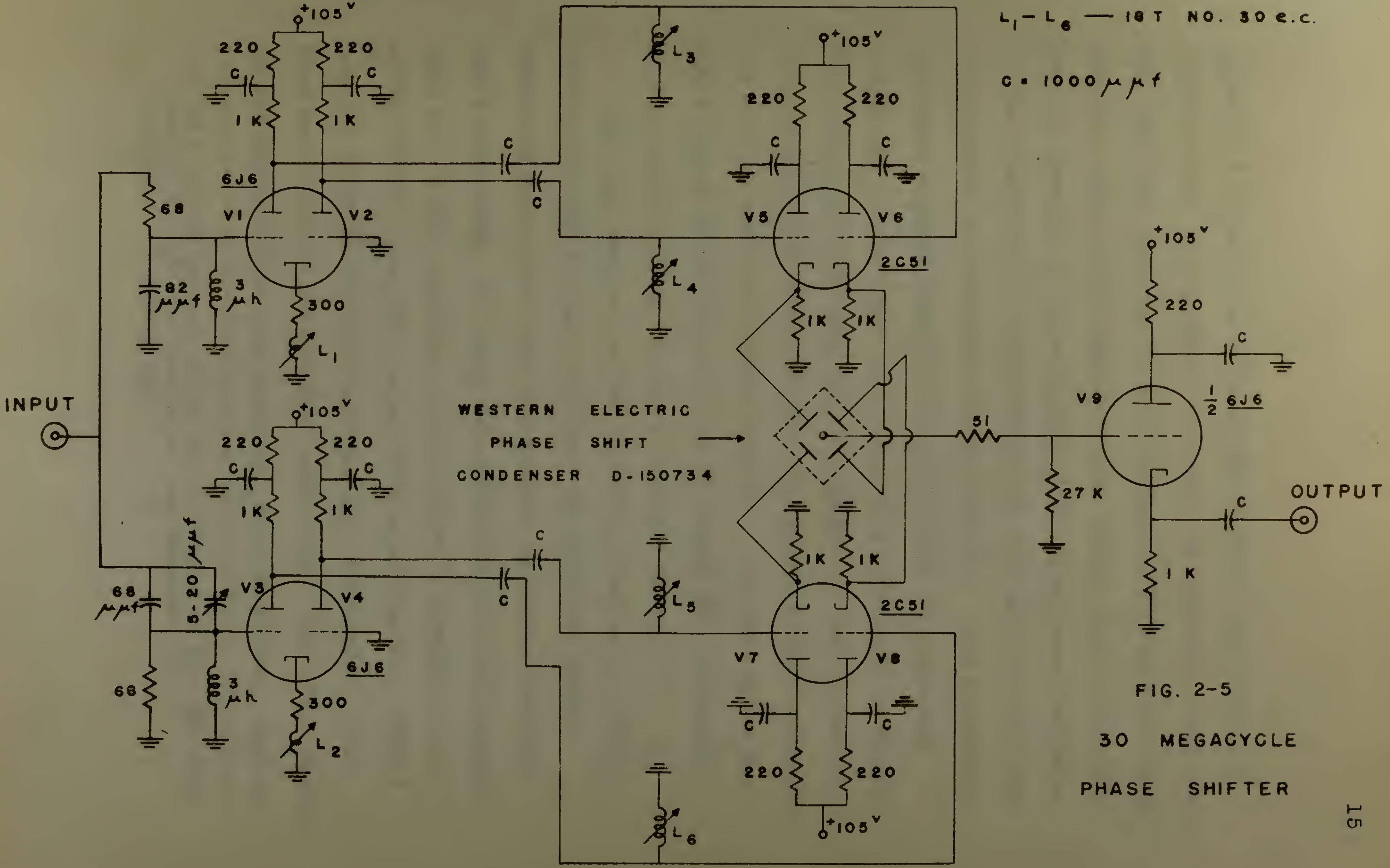
3. This 30 megacycle phase shifter was designed by W. B. Renhult of the Research Laboratory of Electronics at the Massachusetts Institute of Technology.



L1 – L6 — 18 T NO. 30 e.c.

C = 1000 μμf

FIG. 2-5

30 MEGACYCLE

PHASE SHIFTER

signals is varied from zero to 360 degrees, the Lissajous figure on the oscilloscope will make one complete revolution. This fact was utilized in calibrating the 30 megacycle phase shifter, and a block diagram of the system used in the calibration process is shown in Fig. 2-6. There was available in the laboratory a system which had been successfully used to calibrate 100 kilocycle phase shifters. That portion of the block diagram shown in Fig. 2-6 which is contained within the dotted lines was the system previously developed.[4] The problem of utilizing this equipment in the calibration of a 30 megacycle phase shifter was solved by the construction of four additional mixer stages. A General Radio Co. 805-B Signal Generator was used to supply the 29.05 megacycle signal needed for the frequency conversion.

The dial mounted on the shaft attached to the phase shift capacitor was set on zero. An arbitrary small amount of phase shift was introduced, using the 100 kilocycle goniometer, to bring the pattern on the oscilloscope into the desired position, in this case a straight line at 045°-225°. When the phase shift capacitor was rotated through 5.625 electrical degrees, the oscilloscope waveform went through one complete revolution. The dial reading on the phase shifter was recorded, and the process repeated

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4. This system was set up by R. A. Glaser of the Research Laboratory of Electronics at the Massachusetts Institute of Technology.

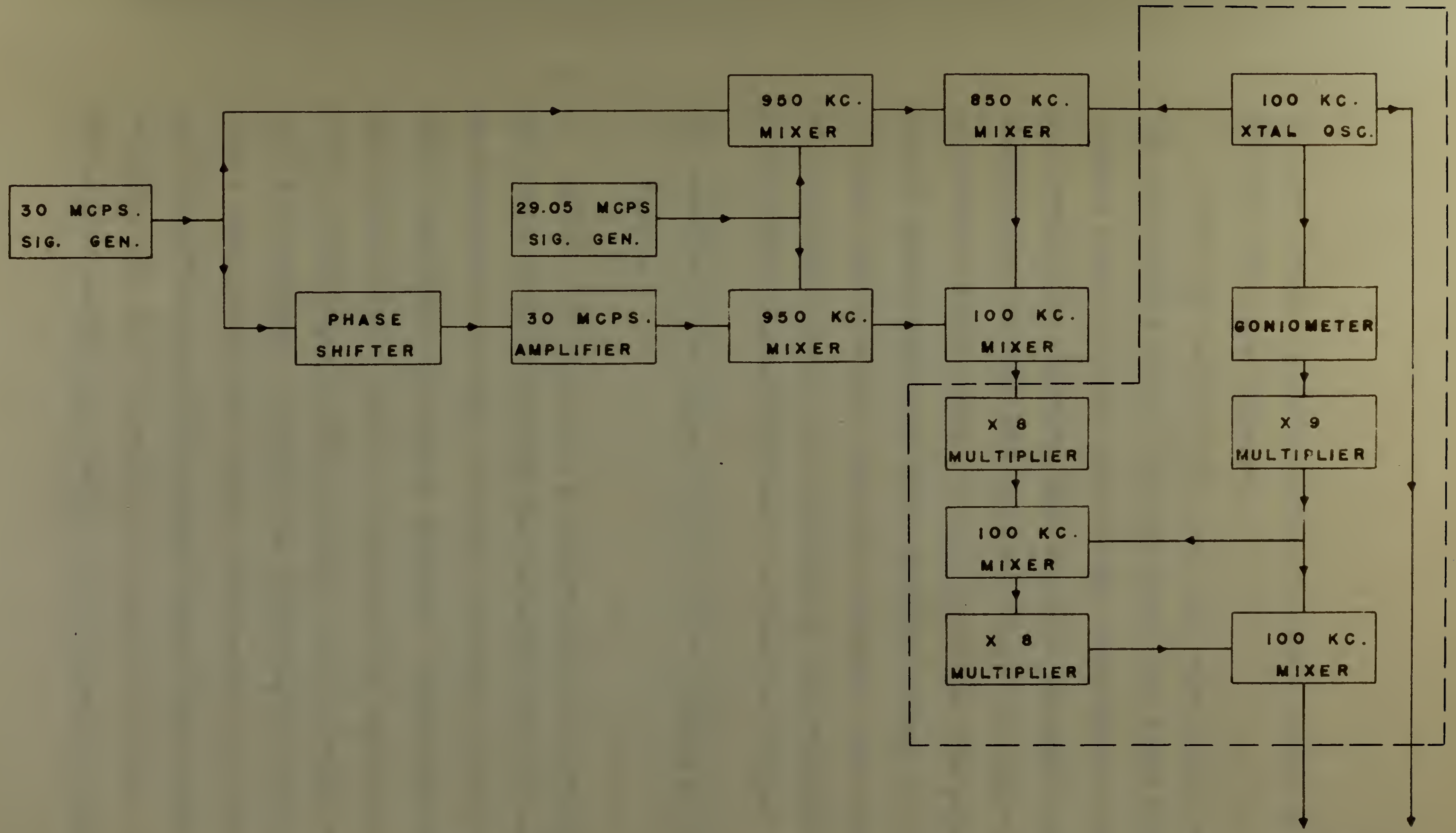


FIG. 2-6
30 MEGACYCLE PHASE SHIFTER CALIBRATION SYSTEM
BLOCK DIAGRAM

63 more times. In this manner, 64 check points on the phase shifter dial were obtained.

After the calibration runs, the known facts regarding the 64 recorded points was that they were 5.625 electrical degrees apart, and the phase shift condenser had made exactly one revolution. Knowing that these 64 recorded points were contained in exactly 360 physical degrees of phase shift capacitor rotation made it possible to use the phase shifter in the investigation of phase detector output as a function of phase shift between the input signals. The actual point of zero phase shift was determined by observing the output of the three phase detectors as a function of dial rotation.

C. Results of the Phase Detector Tests, Using CW Input Signals

Before entering into a discussion of the results of the tests conducted during the investigation, it would be advisable to recall the three principle operations which take place in a phase detector. First, the phase splitting process, usually accompanied by amplification of the input signal which is split into two equal vectors, 180° out of phase. Second, the combining of voltages to form a vector sum and a vector difference, with possibly some amplification of the second input signal before it combines with the two equal and opposite voltages. Third, the actual rectifying process and differential addition

of the rectifier outputs.

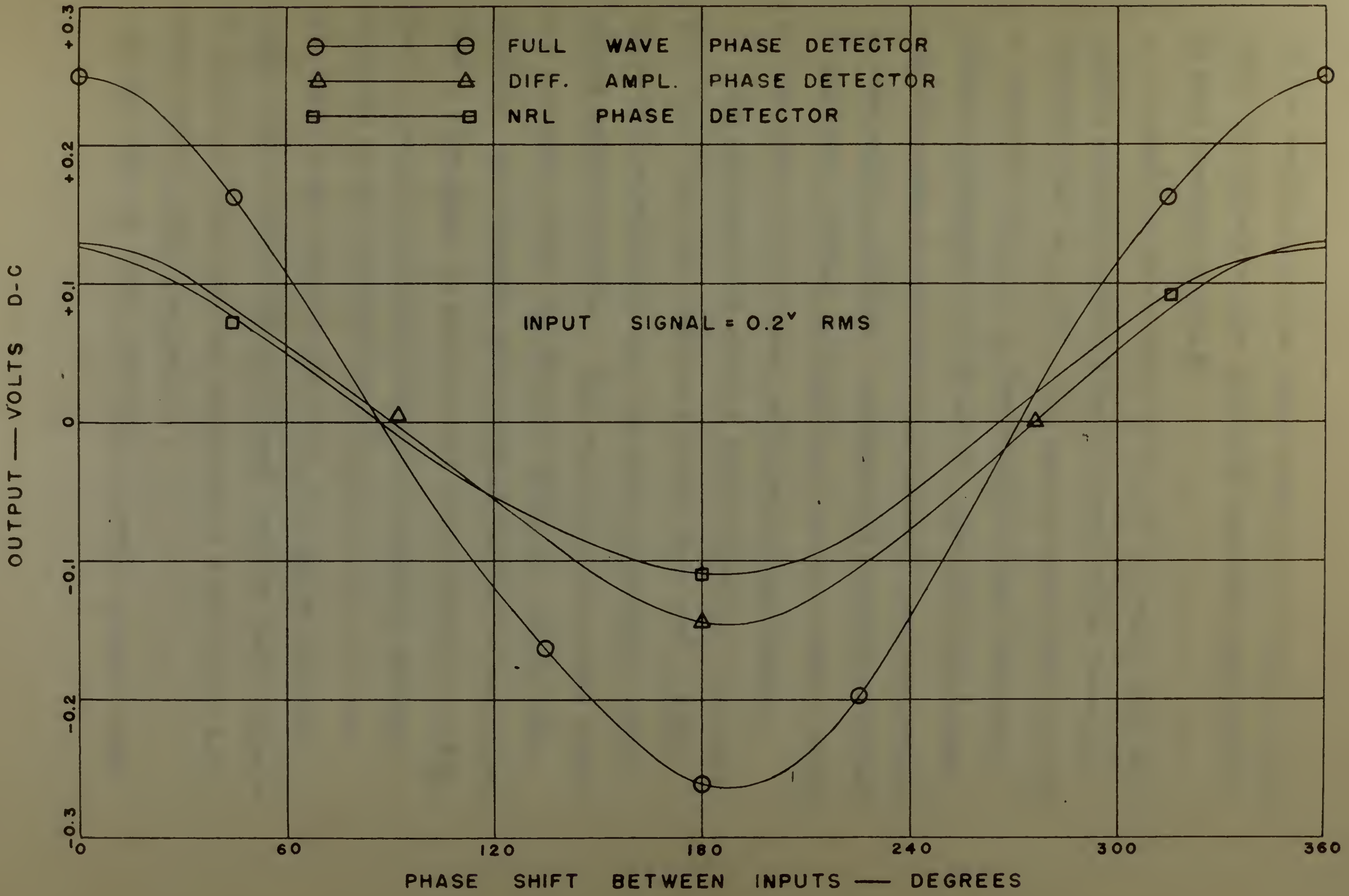
The first tests were made with a 30 megacycle unmodulated CW signal; referring to Fig. 1-1, that portion of the block diagram was in use beginning with the signal generator, up to and including the phase detector. Since the phase shifter had a measured attenuation of 38 db, it was necessary to amplify the output from that unit. A 30 megacycle AN/APS-10 I.F. amplifier strip was used throughout the research project for this purpose.

The gain of the 30 megacycle amplifier was adjusted to produce equal signals at both inputs to the phase detectors. Fig. 2-7 presents a plot of the output of the three phase detectors as a function of phase difference between the inputs. As expected, the amplitude of the output signal from the full wave phase detector was the greatest of the three. This may be attributed to more amplification before the detector stages, and a greater efficiency of detection. The output from the differential amplifier phase detector is slightly larger than that from the NRL phase detector, which is due principally to more gain in the phase-splitting cathode-coupled amplifier.

While the data to be plotted were recorded, the gain of the 30 megacycle amplifier was unchanged. However, the amplitude of the output signal from the phase shifter was not constant, but varied five per cent as a function of phase shift condenser setting. With such a small change

FIG. 2-7

PHASE DETECTOR OUTPUT AS A FUNCTION OF PHASE SHIFT



in the amplitude of the input signal, the amount of phase shift introduced by the AN/APS-10 amplifier was assumed to have remained constant.

A study of the curves in Fig. 2-7 reveals that the maximum negative output from all three phase detectors occurred when $\theta = 187°$. The most logical conclusion to be derived from such an observation is that the phase shifter calibration was in error. The fact that these negative peaks do occur at approximately the same point is encouraging, however. Assuming the error has occured in the phase shifter calibration, the dial setting chosen as the point of zero phase shift was a good choice.

The 30 megacycle carrier input signals to the phase detectors were next modulated 30 per cent with a 1000 cycle per second sine wave, in order to produce a sinusoidal output waveform. This one kilocycle output signal was analyzed, using the General Radio Co. 736-A Wave Analyzer, to determine the harmonic content of the output. Over a wide range in amplitude of input signals, the NRL phase detector output had the lowest harmonic content, followed by the differential amplifier phase detector. For small input signals, the full wave phase detector output was of low harmonic content, but for input signals of over 0.5 volts rms, the output had a high second and third order harmonic content.

One test in which particular interest was expressed

was a study of the phase detector outputs as the ratio of the amplitude of the two inputs was varied from 1:1 to 10:1. For these tests the larger signal was applied to channel "A" and the smaller signal to channel "B"; the signals were then interchanged to put the small signal in channel "A", and the large signal in channel "B".

With a 30 megacycle carrier, modulated 30 per cent at one kilocycle, the amplitudes of the two input signals were varied from 0.1 volts to 1.5 volts rms. The NRL and differential amplifier phase detectors performed equally well under these conditions, but the output from the full wave phase detector was distorted, particularly when large signals were applied to channel "A".

One of the stipulated requirements of the phase detectors was that there must be no output when one of the input signals was zero. Over a range of amplitude of input signal of 0.1 volt to 1.0 volt, applied to either channel, all three phase detectors met this requirement satisfactorily. Such a test stresses careful coil tuning and requires equal voltages at the plates of the phase splitting cathode-coupled amplifiers.

When the frequency of the input signals was 30 megacycles, each detector was balanced to give zero output when $\theta = 90^\circ$. One of the desired facts was an indication of how much frequency shift from the center frequency could be tolerated before the phase detector output,

zero at 30 megacycles, became a measurable quantity. Since the phase shifter was designed to operate only at 30 megacycles, the carrier frequency produced by the signal generator could not be varied with input signals applied to both channels, and yet have the results be of any significance. A signal from the signal generator was applied directly into each channel, and the frequency shifted on either side of 30 megacycles until an output was observed from the phase detector being tested. With all three phase detectors, the frequency of the input signal to either channel could be varied from 28 to 32 megacycles before the output voltage became as large as two per cent of the output when $\theta = 0°$ at the center frequency.

With a modulated 30 megacycle signal applied to both channels of each phase detector, there was no increase in distortion in the output signal and no unbalance at a null condition when the plate supply voltage was varied ten per cent above and below the rated vlaue. No tests were conducted to determine the effects of varying the filament supply voltage.

The efficiency of detection taking place in each phase detector was measured, with the following results:

NRL phase detector--27.3 per cent
Differential Amplifier phase detector--28.7 per cent
Full wave phase detector--33.0 per cent

The computed improvement in detection efficiency for the

full wave phase detector over a half wave detector was $12\frac{1}{2}$ per cent. This value was computed for diode loads of 2.2 K and 24 $\mu\mu f$. The computed value agrees favorably with a measured increase of approximately 15 per cent.

D. Results of the Phase Detector Tests, Using Pulsed Input Signals

After the three phase detectors had been tested using CW and modulated CW input signals, one of the pulsers shown in Fig. 1-1 was connected to the signal generator. The output of a Hewlett Packard Model 200 Audio Oscillator was used to trigger the pulser; the frequency of the audio signal was the pulse repetition rate of the pulser output. A negative output pulse from the pulser was applied to the signal generator, whose output in turn was an envelope of the carrier frequency. Fig. 2-8 is a photograph of the output waveform from the pulser, for a pulse width of 1.5 microseconds. A photograph of the signal generator output is presented in Fig. 2-9. Note the slow decay in amplitude of the oscillations along the trailing edge, although the modulating pulse has a steep trailing edge.

The tests which had been conducted for the CW and modulated CW input signals to the phase detector were repeated with the pulse inputs. None of the three phase detectors tested had a null or zero output where one would

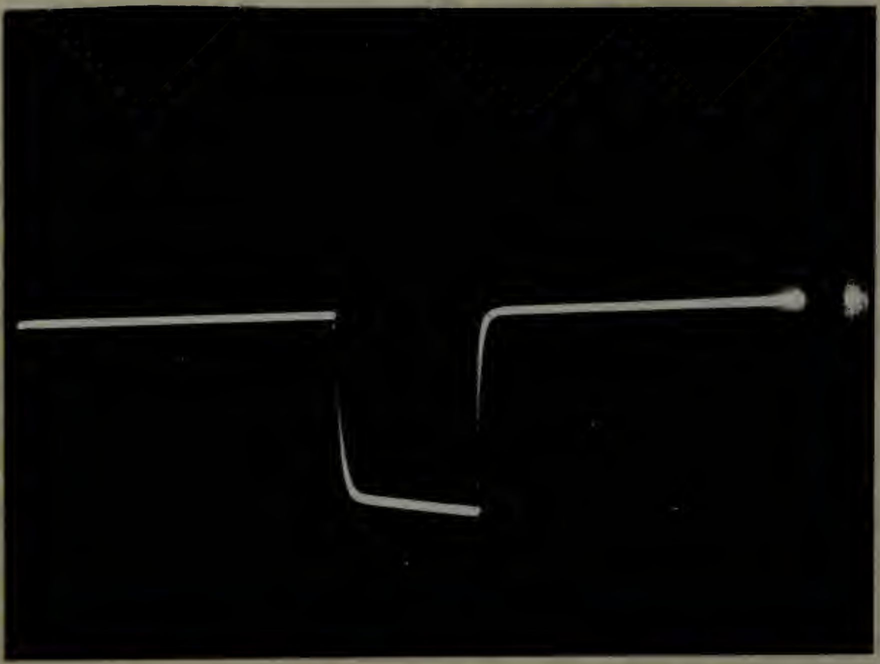


Fig. 2-8 Input pulse applied to signal generator.

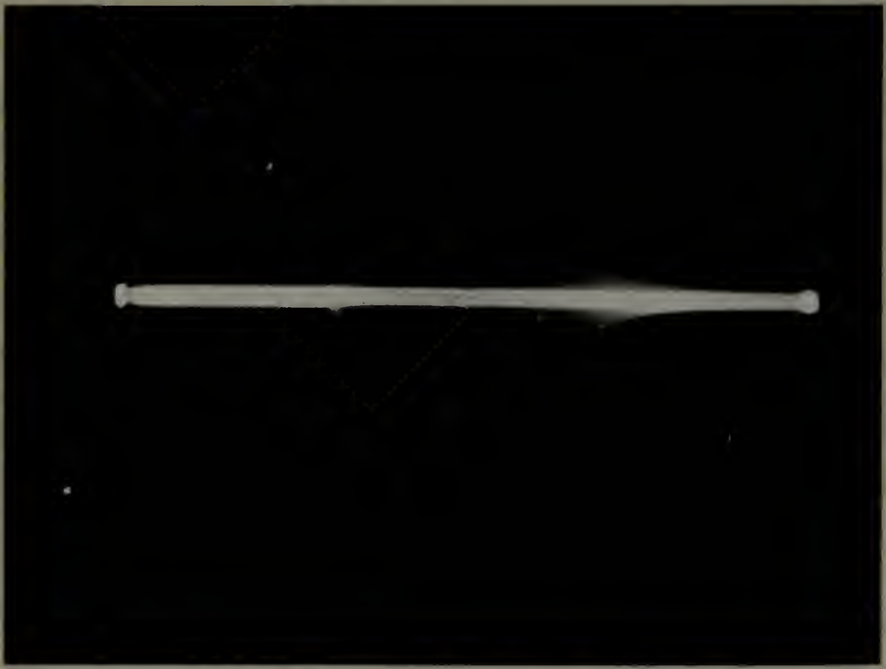


Fig. 2-9 Envelope of signal generator output.

have been obtained using CW input signals. This was particularly true for pulse widths up to five microseconds. No matter what the setting of the phase shifter, there was always a small output indication of both polarities. This output was attributed to the fact that there is a certain amount of frequency modulation at the leading and trailing edges of the signal generator output. The instantaneous deviation in frequency from the center frequency will not be shifted in phase properly in the phase shifter designed to operate only at 30 megacycles.

When the pulse width was increased to 90 microseconds, the center of the pulse produced a satisfactory null. However, at the leading and trailing edges of the pulse, a small voltage "spike" was present. The full wave phase detector produced the best null indications, and of the two half wave detectors, the NRL circuit produced the better nulls.

Much new information was gained from testing the phase detector circuits with pulsed input signals. Of considerable significance was the absence of good, clear-cut null outputs from all three phase detectors. Variation of the pulse repetition frequency from 500 to 3500 pulses per second produced no changes in the wave forms of phase detector output signals. The minimum pulse width obtainable from the General Radio Co. 869-A Pulser was measured as 0.36 microseconds, and with a pulse of that duration,

the output waveform of each phase detector still varied approximately as the cosine function of θ , the phase angle between the two inputs. This minimum pulse width will be referred to again in the next section.

In summarizing the results of the tests conducted on each phase detector, there are specific advantages and disadvantages for each circuit. Although the full wave detector produces a larger output for a given input, and the nulls are better for pulsed input signals, there is a greater percentage of harmonic distortion in the output. The power supply requirements are much greater because of the large number of tubes involved. From the maintenance viewpoint, the full wave phase detector contains nine tuneable coils, which require a great deal of time to line up accurately.

Of the other two phase detectors tested, the results show that the NRL circuit was superior in performance to the differential amplifier phase detector. These two circuits contain the same number of tubes and coils, and require the same amount of time to tune the coils and line up the circuit. From the point of view of compactness, the NRL phase detector may be constructed using only two tubes--a twin triode for the phase splitting cathode-coupled amplifier, and a twin diode for the rectification stage. The addition of a two stage pulse amplifier would produce larger signals than could be

obtained from the vastly more complex full wave phase detector. The phase detector circuit designed by the Naval Research Laboratory is superior to the other two which were investigated.

E. A One Megacycle Model of the Differential Amplifier Phase Detector

The problem of how many cycles of the carrier frequency must be compared before a phase detector can give a reliable indication of the phase relationship existing between the two input signals was stated briefly in the introduction. The answer to this problem could not be obtained when the carrier frequency was 30 megacycles. With the minimum pulse width available from the pulser 0.36 microseconds, each pulsed input signal to the phase detector would consist of approximately 11 cycles of the carrier frequency. Since each phase detector produced an output signal which varied satisfactorily as a function of θ when the input pulse width was a minimum, the answer to the problem could not be obtained at 30 megacycles, with the existing equipment.

A one megacycle differential amplifier phase detector was constructed from the schematic wiring diagram given in Fig. 2-3. Resistor values were not changed, but all capacitor and coil values were multiplied by a factor of 30, since frequency was divided by 30 and time multiplied

by a factor of 30. Additional capacitors were added to simulate the effect of tube and wiring capacitances at one megacycle.

To avoid the necessity of constructing a new one megacycle phase shifter, the new phase detector was tested using the system presented in Fig. 2-10. The schematic wiring diagram of the mixers is presented as Fig. 2-11.

In operation, the output of the 30 megacycle signal generator was a pulse of carrier energy, while the 29 megacycle signal generator output was a CW signal. The selectivity of the tank circuit in each mixer was such that there was no output from the mixers when the 30 megacycle signal was not applied.

The amount of energy available in the pulse spectrum of the input signal to the phase detector which reaches the diodes for rectification is dependent upon the band width of the phase splitting cathode-coupled amplifier. For purposes of comparison, the band width of this amplifier in the 30 megacycle differential amplifier phase detector was measured to be 16 megacycles. In the one megacycle phase detector, the corresponding band width was measured as 560 kilocycles. For an exact comparison, the band width should be 533 kilocycles.

One limitation encountered in using the system shown in Fig. 2-10 was the narrow band width of the mixer stages. In order to have a useable output, the computed **Q** of the

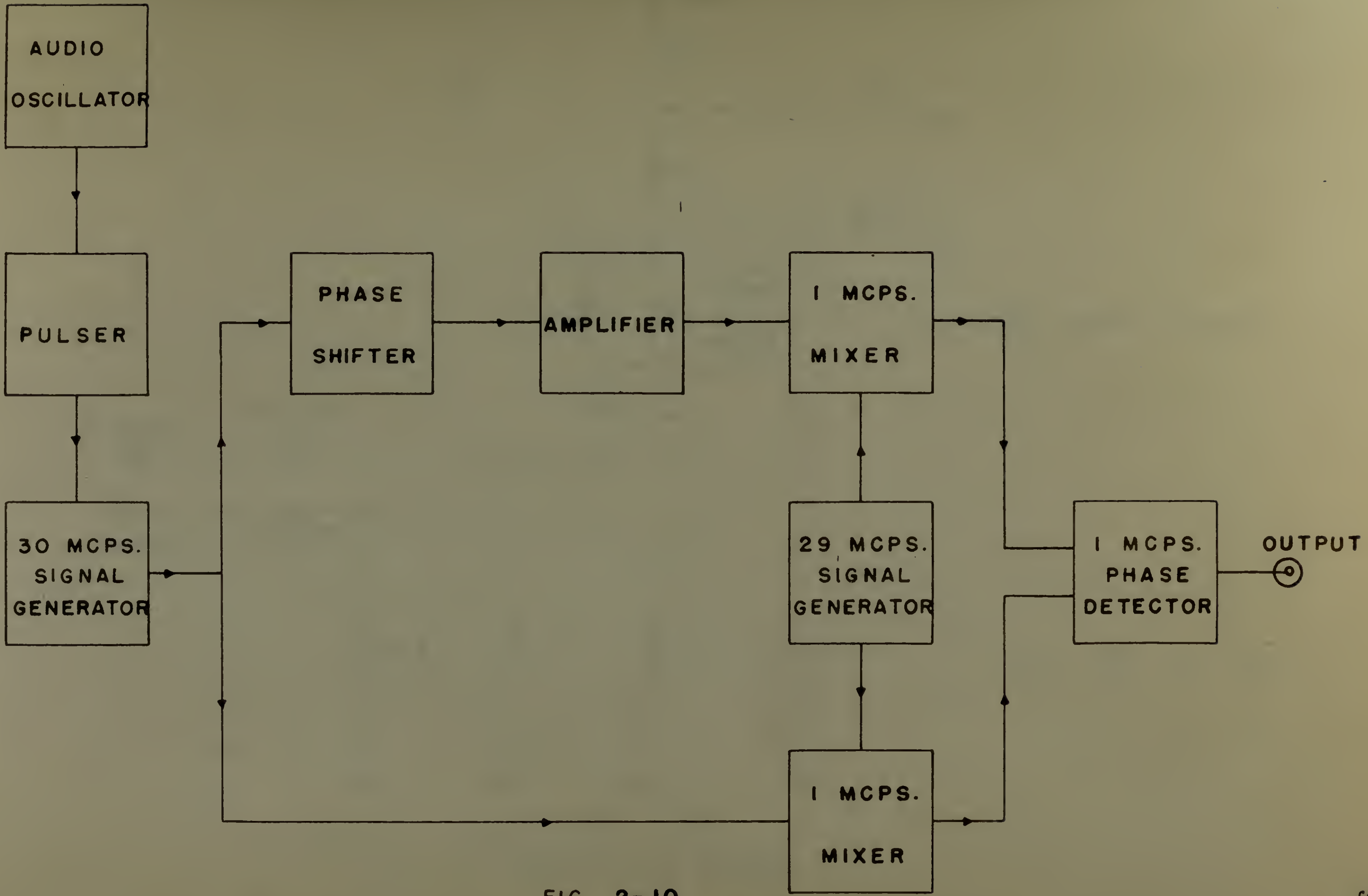
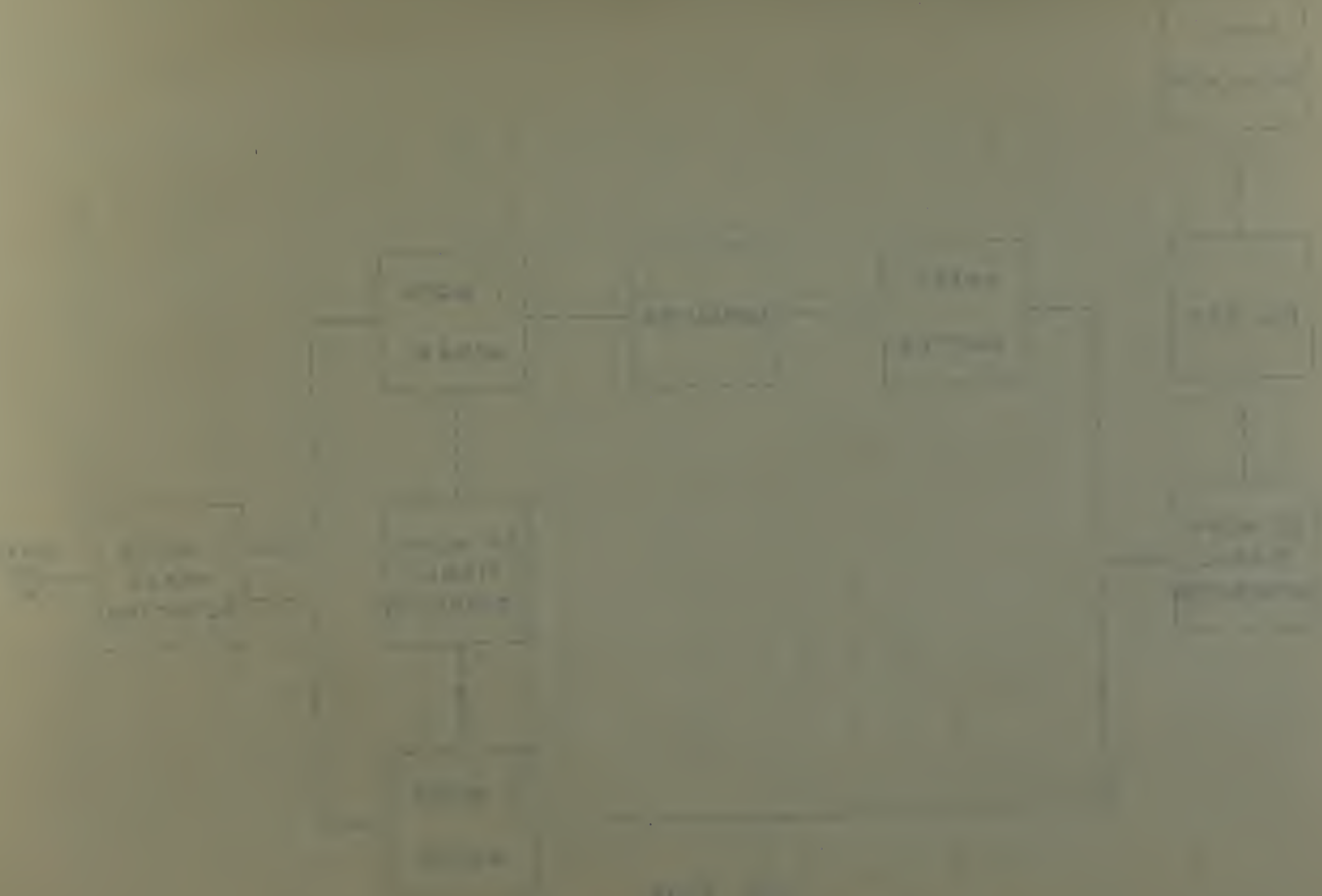


FIG. 2—10

PHASE DETECTOR TEST SYSTEM —— BLOCK DIAGRAM



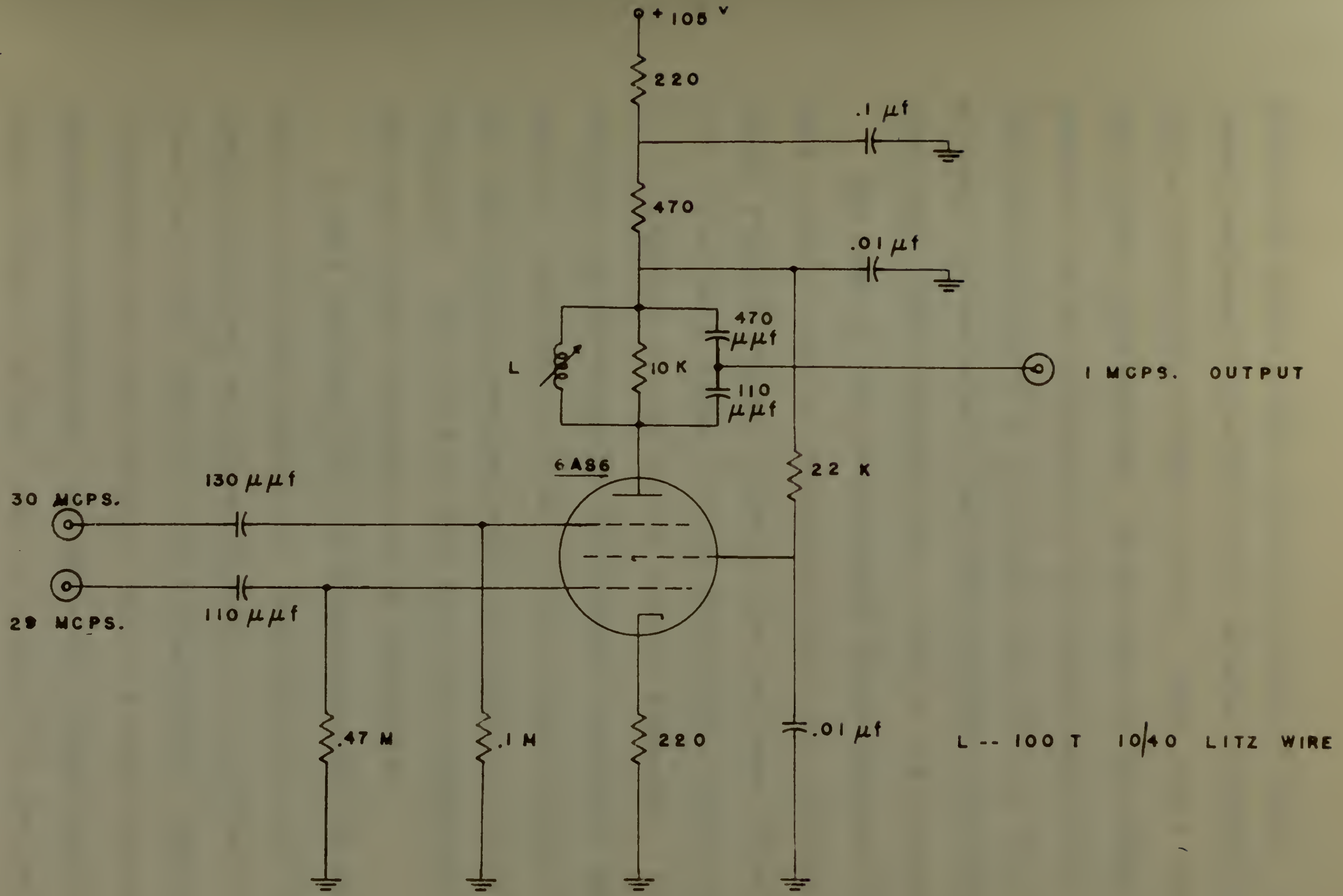


FIG. 2–11
I MEGACYCLE MIXER

mixer tank circuits was fixed at a value of five. The actual measured band width of the mixers was 165 kilocycles, indicating a value of $Q = 6$. With such a narrow band width, approximately 25 per cent of the energy contained in the spectum of a six microsecond pulse would not be passed by the mixer. In spite of this loss of energy in the mixer, the phase detector operated satisfactorily for a minimum pulse width of six microseconds.

The test on the one megacycle phase detector indicated that a pulse width of six microseconds was sufficient to insure reliable output signals from the phase detector. In a pulse whose width was six microseconds there would be six complete cycles of the carrier frequency. By analogy, the 30 megacycle differential amplifier phase detector would also provide reliable output signals when the input pulse contained only six cycles of the carrier frequency. This would be true for a 0.2 microsecond pulse, when the carrier frequency was 30 megacycles.

A more judicious line of reasoning could be obtained from the following procedure. Construct phase shifters, tuned amplifiers, and phase detectors to operate at frequencies of one, five, ten and 15 megacycles, thereby eliminating the mixer stages. With all units properly frequency-proportioned, determine the minimum input pulse width necessary in each case to produce the desired output. By means of a suitable process of extrapolation, a good

indication of the minimum input pulse width necessary to produce satisfactory operation of the 30 megacycle phase detector could be obtained.

The steps outlined in the preceding paragraph would require a considerable amount of time for constructing and testing the units. Such a program could well be made the basis for a more complete investigation of pulsed high frequency phase detectors.

CHAPTER III

THE PULSE-INTEGRATING CIRCUIT

The primary function of the pulse-integrating circuit is to facilitate the accurate measurement of the envelope frequency of the phase detector output pulses. This envelope frequency is the cyclic variation in the amplitude of the phase detector output pulses if there is a constant rate of change of phase between the two inputs to the phase detector. In the experimental system, the rate of change of phase was produced by attaching a small electric motor to the shaft of the phase shift capacitor in the phase shifter.

Pulse-integrating circuits are a comparatively recent development, and serve to stretch a pulse in time so that its amplitude can be closely observed and this information handled with greater ease in subsequent circuits. A majority of the pulse-integrating circuits developed accept only positive input pulses, but for stretching the output pulses from a phase detector, a circuit which will accept either positive or negative input pulses must be used.

A. Principle of Operation.

The principle upon which these circuits operate is as follows, explained with the aid of Fig.3-0. With the switch S closed, a pulse from the source charges capacitor C to a

voltage equal to that of the pulse peak. The time constant of the charging path is very short. At the instant of termination of the input pulse, switch S is opened, and the charge stored on C must leak off through an output circuit whose input impedance is very high. As a result, the time constant of the discharge path of the storage capacitor C is very long, and the capacitor tends to retain the stored charge until the application of the succeeding pulse. Just prior to the arrival of the next pulse, switch S is closed, and the process repeats itself.

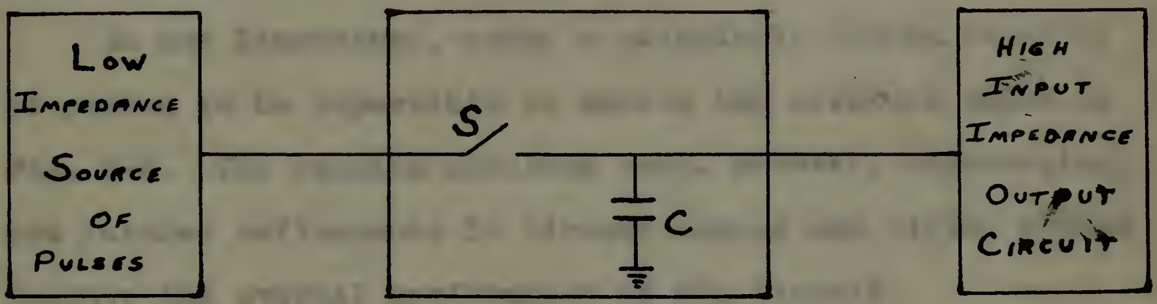

Low Impedance Source of Pulses
S
C
High Input Impedance Output Circuit

Fig. 3-0 Basic pulse-integrating circuit--block diagram

Loss of the stored charge from the main capacitor between the end of one pulse and the beginning of the next pulse will be referred to as voltage "droop". The greater the repetition rate of the input pulses, the smaller will be the loss of energy due to the voltage "droop".

For a clearer understanding of the operation of a pulse-integrating circuit, refer to the diagrams on the

following page. Fig. 3-1 represents a typical output waveform from the phase detector, such as would be the case if the pulse repetition frequency were 600 pulses per second and the envelope frequency were 50 cycles per second. The time interval between pulses is the reciprocal of the pulse repetition frequency. Fig. 3-2 represents the idealized output waveform from a pulse-stretching circuit, in that there is no droop in the charge stored on the capacitor during the interval between pulses. With a minimum of filtering, a good sinusoidal waveform could be obtained from such an output.

In the laboratory, using a relatively simple circuit, it proved to be impossible to obtain the waveform shown in Fig. 3-2. The results obtained were, however, encouraging, and further refinements in circuit design and wiring should improve the overall performance of the circuit.

B. The Circuit Tested in the Laboratory.

A study of the history of pulse-integrating circuits revealed that most of the circuits had been designed to accept input pulses of one polarity only, usually positive. Their principal use was in stretching out the video pulses in radar sets for a number of different purposes. The circuit chosen for detailed study is not original with the author.[1] Of primary importance are the ability of this

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[1] This pulse-integrating circuit is credited to Mr. B. M. Oliver of the Bell Telephone Laboratories.

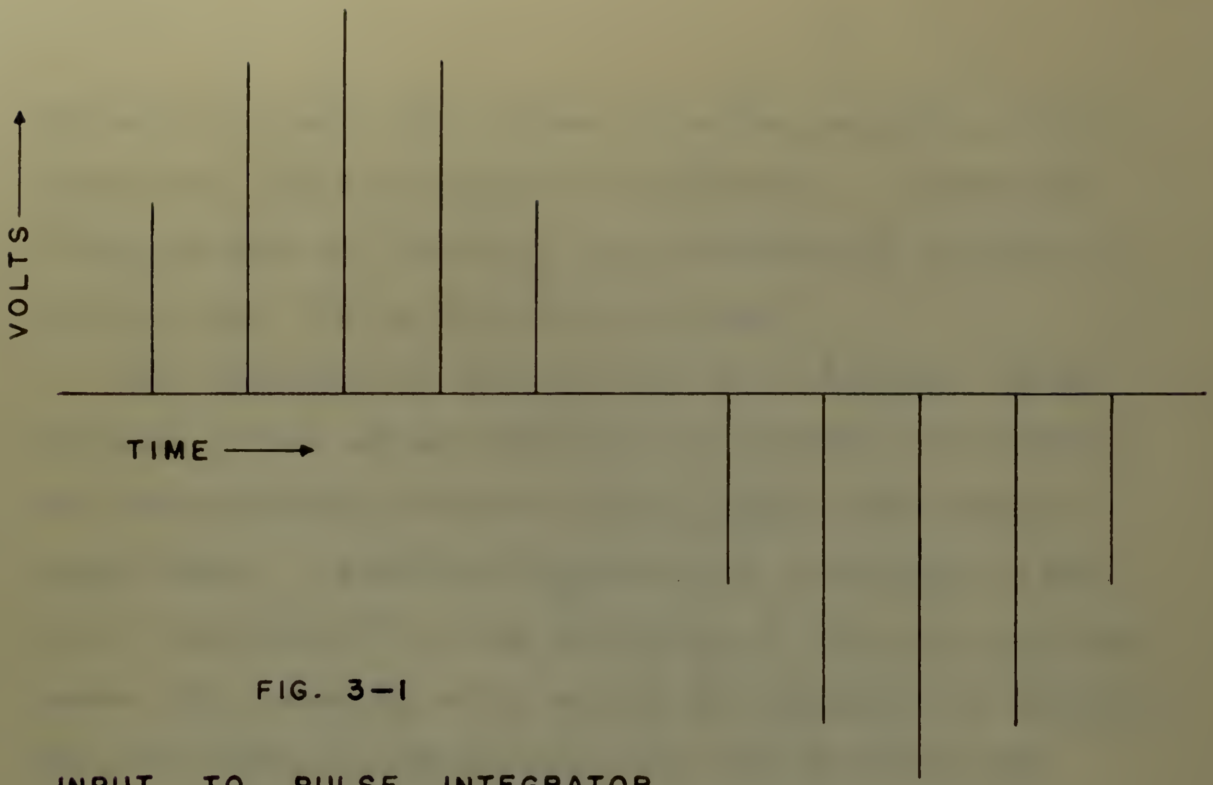


FIG. 3-1

INPUT TO PULSE INTEGRATOR

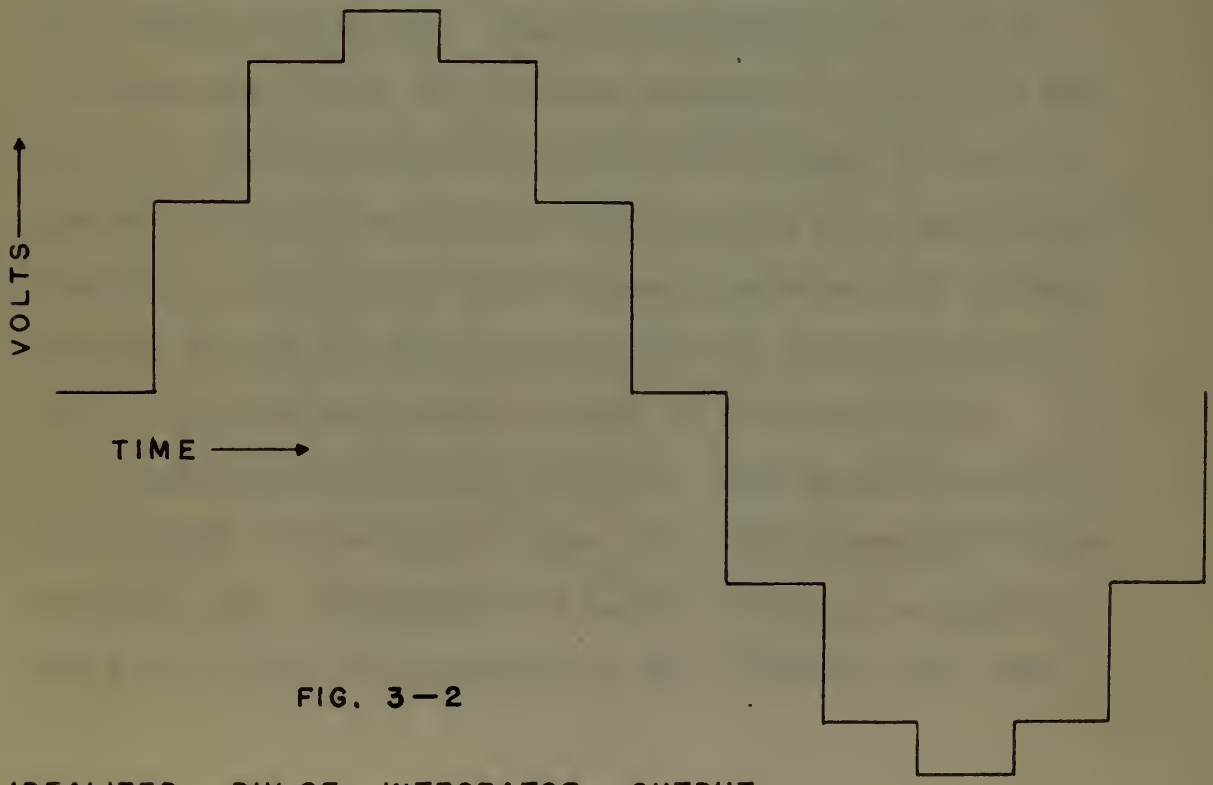


FIG. 3-2

IDEALIZED PULSE INTEGRATOR OUTPUT

EXIT

[illegible]

EXIT

[illegible]

circuit to accept input pulses of either polarity, its simplicity, and the economy of components. A schematic wiring diagram of the diode pulse-integrating circuit is shown in Fig. 3-3 on the following page.

The operation of this circuit is as follows. With no input signal and no clamping gate applied, the diodes are non-conducting because of the negative bias voltage across them. A positive clamping gate is applied to the pulse transformer T1. The amplitude of the gate appearing across the secondary of T1 should be sufficient to overcome the bias voltage, and current will flow in all of the diodes. Let us assume identical tubes, such that the current flowing in each diode is the same.

With all the diodes conducting equally, a positive input pulse decreases the voltage across V1 and increases the voltage across V2. The current through V2 and V3 is increased, while the current through V1 and V4 is decreased. The difference in currents through V3 and V4 produces a positive charge stored on the main capacitor C. Similarly, a negative input signal increases the current through V1 and V4 while decreasing the current through V2 and V3, and the charge stored on C is negative.

Because the clamping gate has been applied prior to the arrival of the input pulse, the time constant of the charging path of capacitor C is very short. As soon as the input pulse has terminated, the clamping gate ends.

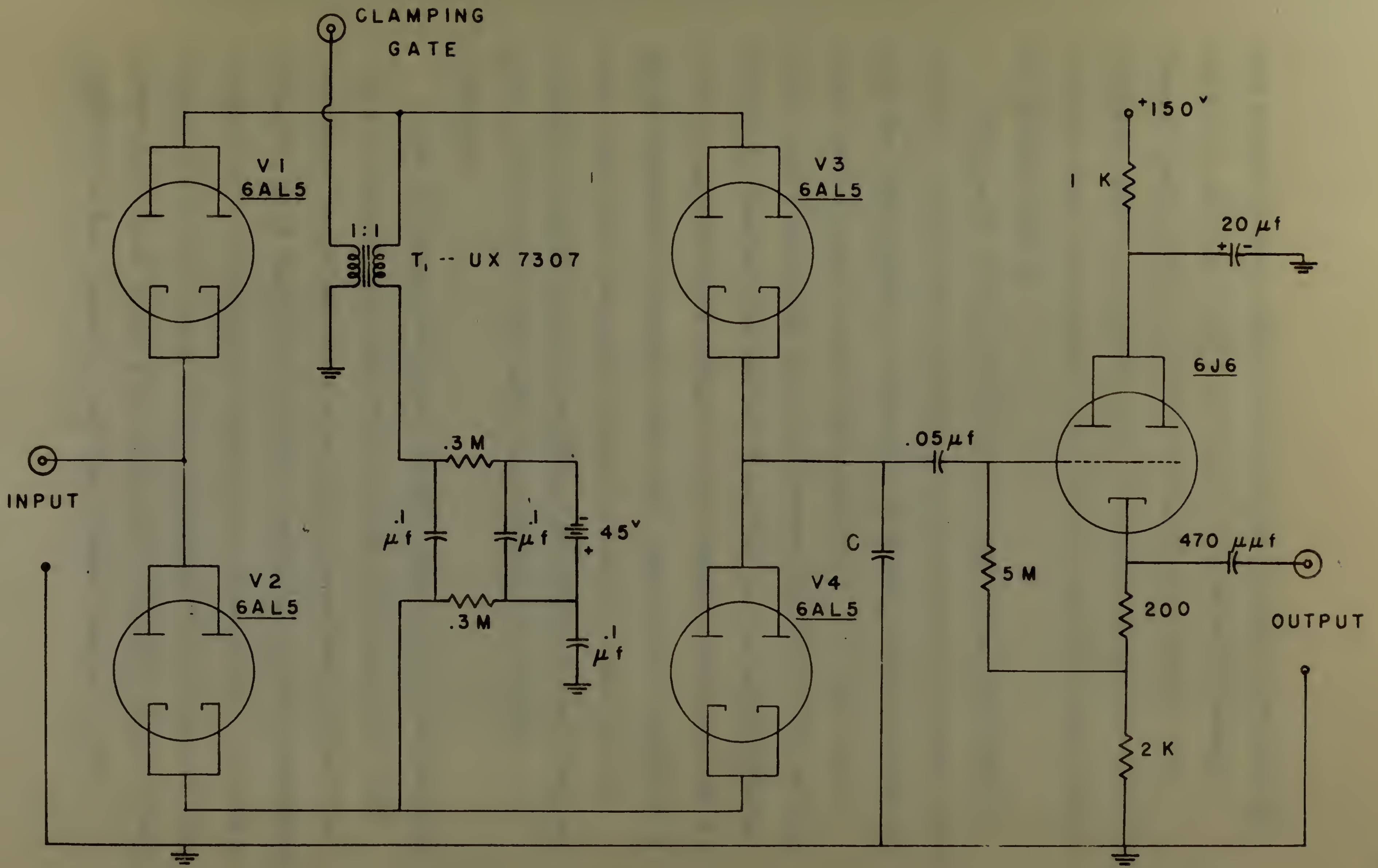
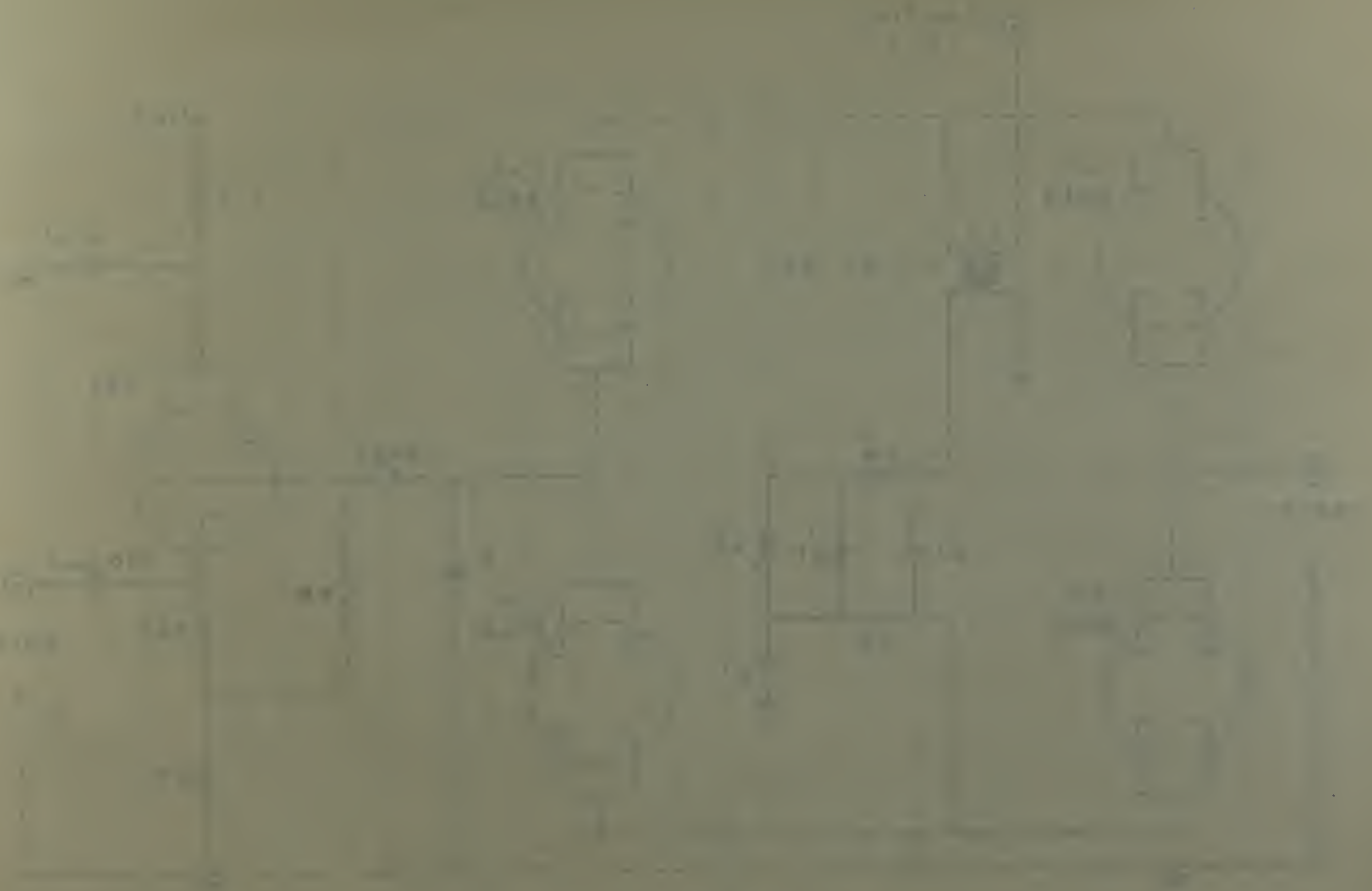


FIG. 3—3

PULSE INTEGRATING CIRCUIT



The negative bias voltage across the diodes prevents conduction, and the charge stored on C gradually decays toward zero during the interval between pulses. The cathode follower output stage has been designed to provide a high input resistance in an effort to reduce the leakage of charge from C.

The most critical feature of the pulse-integrating circuit is the time relationship between the clamping gate and the input pulse. Generally speaking, the duration of the clamping gate is not too important. If the input pulse has a duration of one microsecond, the width of the clamping gate may be varied from two to ten microseconds with no appreciable change in the output waveform. It is most important, however, that the input pulse arrive at a time such that the pulse width is exactly equal to or slightly less than the remaining duration of the clamping gate. The reason for this exact timing is readily apparent.

Let us assume an input pulse width of one microsecond and a clamping gate duration of five microseconds, with the input pulse set to arrive two microseconds after the clamping gate has been applied. With the diodes conducting, capacitor C will store a charge, and the voltage developed across C will be equal to the amplitude of the input pulse. After the input pulse has ended, the clamping gate is still applied to the circuit, and the diodes remain in the

conducting state. The short time constant charging path for C still exists, and serves to provide a short time constant discharge path for C. During the remaining two microseconds of the clamping gate duration, all of the charge stored on C has leaked off through the low impedance source of the input pulses.

On the following page the waveform of a three microsecond clamping gate applied to the transformer T1 is shown in Fig. 3-4, while a typical positive input pulse one microsecond in width is presented in Fig. 3-5.

Fig. 3-6 is a photograph showing the superposition of the clamping gate and the input pulse, positive in this case. The assumed conditions described in a previous paragraph are clearly illustrated, except that the photograph portrays a one microsecond pulse superimposed in approximately the center of a three microsecond gate. This picture is of the voltage waveform existing at the plates of V1 and V2.

When the clamping gate causes the diodes to conduct, and the input pulse does not arrive until served microseconds later, any charge stored on the capacitor from the preceding pulse is immediately dissipated through the short time constant discharge path. With the arrival of the next pulse, the capacitor assumes a new charge, and the clamping gate must be terminated immediately to prevent the undesirable loss of charge stored by the new

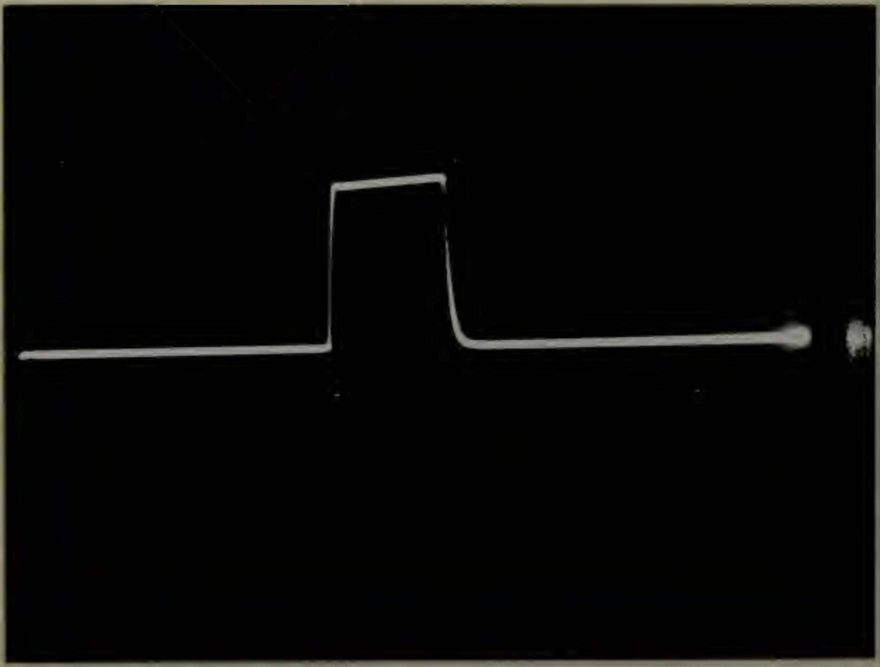


Fig. 3-4 Waveform of clamping gate

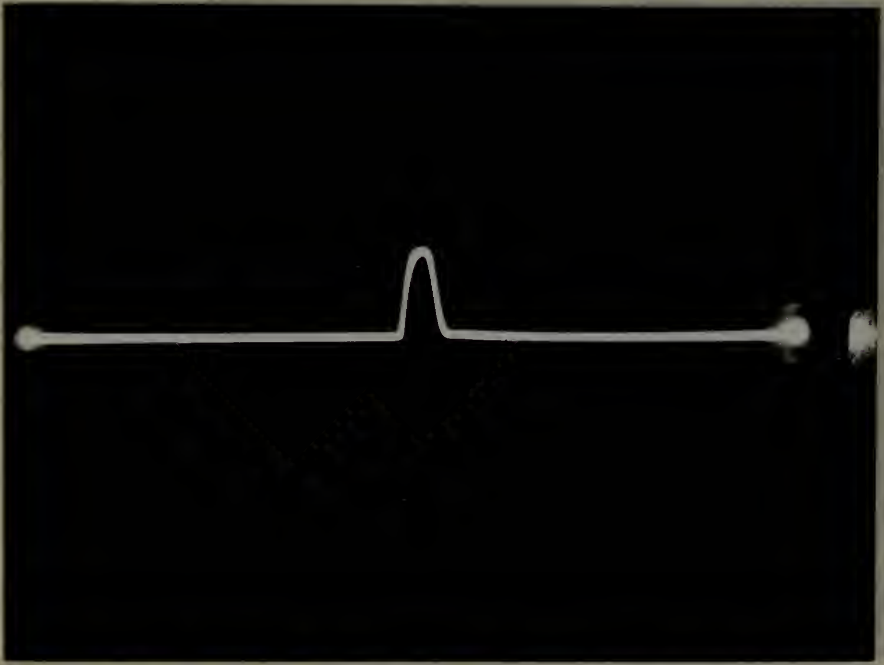


Fig. 3-5 Waveform of one microsecond input pulse

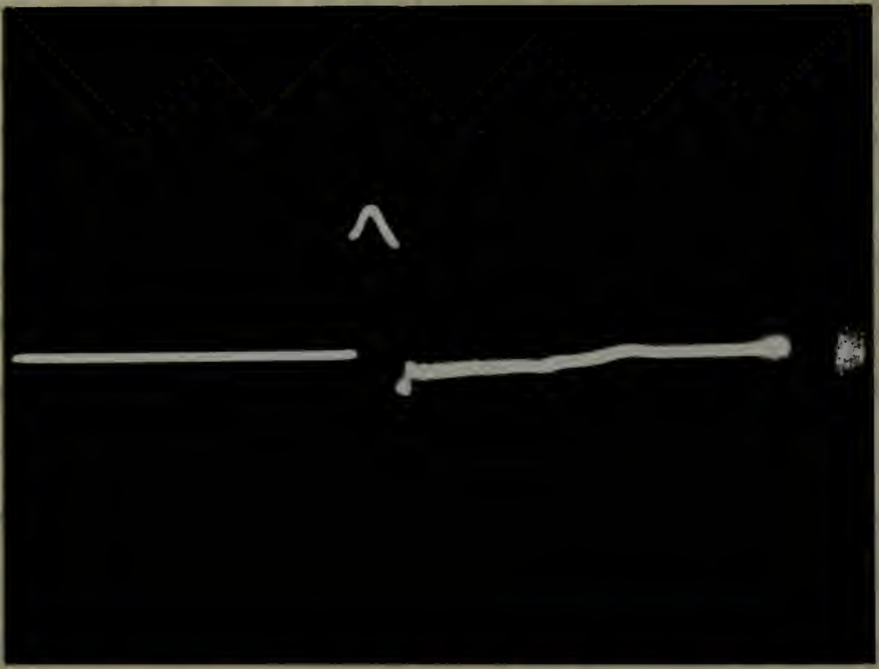


Fig. 3-6 Superposition of clamping gate and positive input pulse.

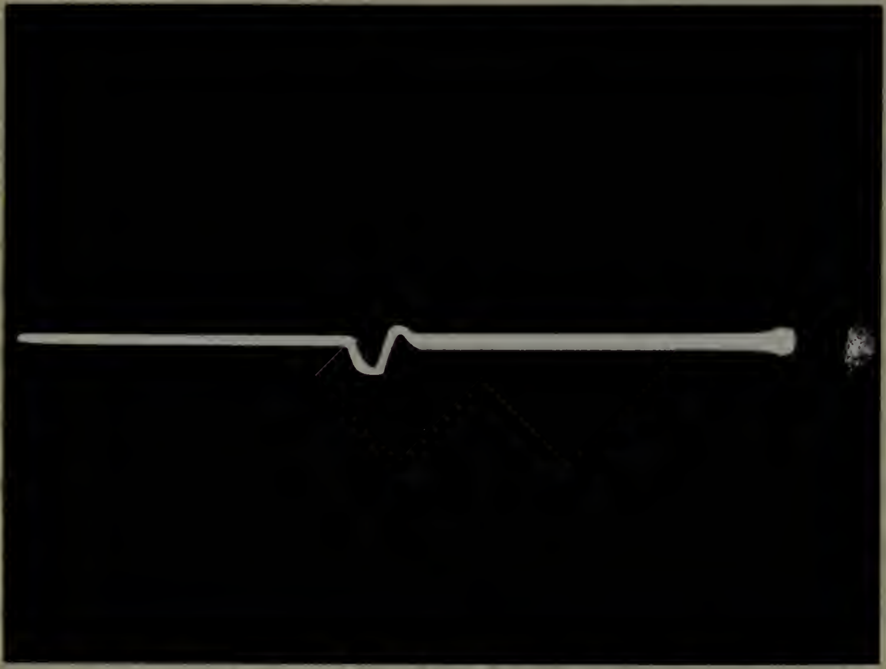


Fig. 3-7 Voltage waveform at input to cathode follower.

input signal. Fig. 3-7 illustrates this action clearly. A positive charge has been stored on the capacitor prior to the arrival to the clamping gate. This photograph shows the sudden exponential decay of the voltage across C when the clamping gate arrives, the new positive input pulse, and a slight loss in capacitor charge before the clamping gate is terminated. Fig. 3-7 does not represent the optimum position of the input signal relative to the clamping gate. The photograph was taken to substantiate the preceding statements. For the smallest loss of stored information, the clamping gate should be terminated before there is any discharge from the capacitor, once it has been charged to the level of the input pulse. In the laboratory, the circuit operated satisfactorily when the input pulse and the clamping gate were of the same duration.

C. Design Considerations.

One of the more desirable features of the circuit is the manner in which the clamping gate is applied. With no input pulse, and a well-balanced circuit, no signal will appear at the plates of V3 and V4 when the clamping gate is present. This action reduces the amount of undesirable noise voltage which would appear at the filter output.

The optimum size of the storage capacitor C must be considered carefully. If the input pulse source impedance is 300 ohms, and the impedance of each conducting diode is

100 ohms, the impedance in the charging path is approximately 500 ohms. With an input pulse width of one microsecond, the maximum possible value of C is 500 $\mu\mu f$, if the voltage across C is to approach within 2 per cent of the amplitude of the new input pulse. If the size of C is increased to 1000 $\mu\mu f$, the voltage across C will change only 86 per cent of the total value. This was observed in the laboratory when capacitors of various sizes were tried.

However, the size of C plays a vital part in the amount of voltage droop which can be tolerated during the interval between pulses. The charge stored on C can leak off through several paths, principally the input resistance to the cathode follower stage. Assuming a good capacitor with a small power factor and no loss across the diodes, the resistance of the discharge path would equal approximately the input resistance of the cathode follower. The computed resistance is 25 megohms and if C = 500 $\mu\mu f$, the time constant of the discharge path is 12,500 microseconds. With a pulse repetition frequency of 1000 pulses per second, 7½ per cent of the charge stored on C would leak off before the next pulse arrived. The observed voltage droop in the laboratory at a pulse repetition frequency of 1000 pulses per second was approximately 12½ per cent, indicating that the actual input impedance to the cathode follower was not as high as the computed

value. A value of C = 500 μμf proved to be the optimum size in the experimental circuit.

In actual practice, there will be very large leakage resistances across the diodes and the capacitor, so the magnitude of the cathode follower input impedance should be increased as much as possible, and yet have a flexible cathode follower output stage. Increasing the size of C would decrease the droop, but the value of this capacitor is also governed by the width of the input pulse, as explained previously. The most practical solution would be an increase in the pulse repetition frequency, but in many cases this is not desirable.

The amplitude of the clamping gate produced across the secondary of T1 should be at least four times the amplitude of the largest input pulse to be handled, while the magnitude of the negative bias voltage should be at least twice the amplitude of the largest input pulse. When the clamping gate overcomes the fixed bias voltage, the potential across each diode should be sufficiently large to prevent any diode from being cut off by the largest input signal. If the amplitude of the largest signal is 10 volts, at least a 20 volt bias source and 40 volt clamping gate should be used. The large bias voltage also prevents a discharge of the charge stored on C back through the diodes.

The principal disadvantage of the circuit is the fact that the diodes, pulse transformer and bias source are all

floating with respect to ground. Wiring capacitance may prove to be the most troublesome, although in the laboratory the negative bias source was located outside the experimental chassis with no ill effects.

Replacement of parts did not affect the operation of the circuit, since no component has a particularly critical value. Neither tube replacement nor a different transformer affected the amplitude or waveform of the output.

In summarizing the performance of the pulse-integrating circuit which was investigated, the operational limitations are enumerated below. First, the circuit requires a critical time relationship between input pulse and clamping gate. Second, some compromise must be reached as to the minimum pulse width which can be stretched and the amount of voltage droop which can be tolerated. Third, the majority of the components comprising the circuit are floating with respect to ground. Fourth, the circuit is insensitive to input pulses of small amplitude, i.e., less than one volt. These limitations are accepted in view of the fact that the circuit accepts input pulses of either polarity equally well.

D. Suggestions for Further Work.

Another method of stretching pulses was proposed and rejected because of its complexity. The input pulses would be applied to 2 multivibrators, one to be triggered

by the positive pulses and the other to be triggered by negative pulses. The output gate from each multivibrator would have the same polarity as the input pulse which triggered it. The amplitude of the output gate would also be proportional to the amplitude of the input pulse. Duration of the output gates would be adjusted to slightly less than the interval between pulses.

This method might be developed into a useful pulse-integrator, but the problem of biasing the multivibrators so that an input pulse triggered only one multivibrator would be difficult, particularly for pulses of small amplitude. Where circuits of greater complexity are not objectionable, such a system might be the best method of overcoming undesirable voltage droop.

CHAPTER IV

THE OPERATION OF THE ENTIRE SYSTEM

The equipment shown in block diagram form in Fig. 1-1 was connected as indicated and placed in operation. A two stage pulse amplifier whose schematic wiring diagram is given in Fig. 4-2 was incorporated into the system when it was discovered that the pulse-integrating circuit was insensitive to the small amplitude output pulses from the phase detector. The gain of the pulse amplifier was adjusted for each phase detector used, since the outputs of the three different phase detectors were not equal.

With the major portion of the thesis research devoted to 30 megacycle phase detectors and the pulse-integrating circuit, the design of the best possible filter network was not attempted. A simple RC filter, shown in Fig. 4-3, was used to smooth out the output waveform from the pulse-integrating circuit. An attenuation versus frequency characteristic of this filter is shown in Fig. 4-4. A low-pass LC filter with a cutoff frequency of 100 cycles per second would require chokes of considerable size, and it was felt that time would be better spent on other phases of the system rather than the design and construction of a good filter.

The audio amplifier contained in the Model 300 Ballantine Electronic Voltmeter was used to amplify the

sinusoidal output waveform from the filter. Although this amplification was not absolutely necessary, it was used to present an enlarged pattern on the cathode ray oscilloscope for closer inspection.

The small electric motor attached to the phase shifter was briefly mentioned in the previous chapter. The operating speed of this a-c motor could be varied only by changing the line voltage, and a speed of from 2000 rpm to 3100 rpm was possible with this arrangement. Thus the frequency of the filtered output from the pulse-integrating circuit could be varied from approximately 37 cycles per second to 51 cycles per second. As the speed of the motor was varied, the change in output frequency was readily observed on an oscilloscope used to view the output from the audio amplifier.

Variation of the pulse repetition frequency had an important effect on the output waveform observed. When the pulse repetition frequency was low, i.e., 500 pulses per second, the effect of droop during the interval between pulses could not be completely smoothed out by the filter. Fig. 4-1 consists of three photographs taken of the audio amplifier output waveform at a frequency of 50 cycles per second, for pulse repetition frequencies of 1000, 2000, and 3000 pulses per second. These pictures were taken with a pulse width of one microsecond and a clamping gate width of three microseconds, with the pulse

set to arrive during the last one microsecond of the clamping gate duration. The higher the pulse repetition frequency, the more closely the waveform approaches a true sine wave.

A General Radio 736-A Wave Analyzer was used to measure the harmonic content of the audio amplifier output waveform for different pulse repetition frequencies. The curves plotted in Fig. 4-5 corroborate the photographs in Fig. 4-1 in that increasing the pulse repetition frequency decreases the percentage of pulse repetition frequency components appearing in the output. Low-order harmonics present due to distortion in the envelope of the phase detector output can not be reduced by increasing the pulse repetition rate.

The primary reason for connecting all of the equipment shown in Fig. 1-1 has been the accurate measurement of the phase detector output pulse envelope frequency. In this manner the rate of change of phase between the two inputs to the phase detector can be measured. For the best operating performance, the output waveform should be as nearly sinusoidal as possible. Some distortion will be introduced by the phase detector, and high frequency components will be added in the pulse-integrating circuit. Additional work to increase the input impedance of the cathode follower output stage of the pulse integrating circuit and the design of a better filter for smoothing purposes should improve the output waveform noticeably.

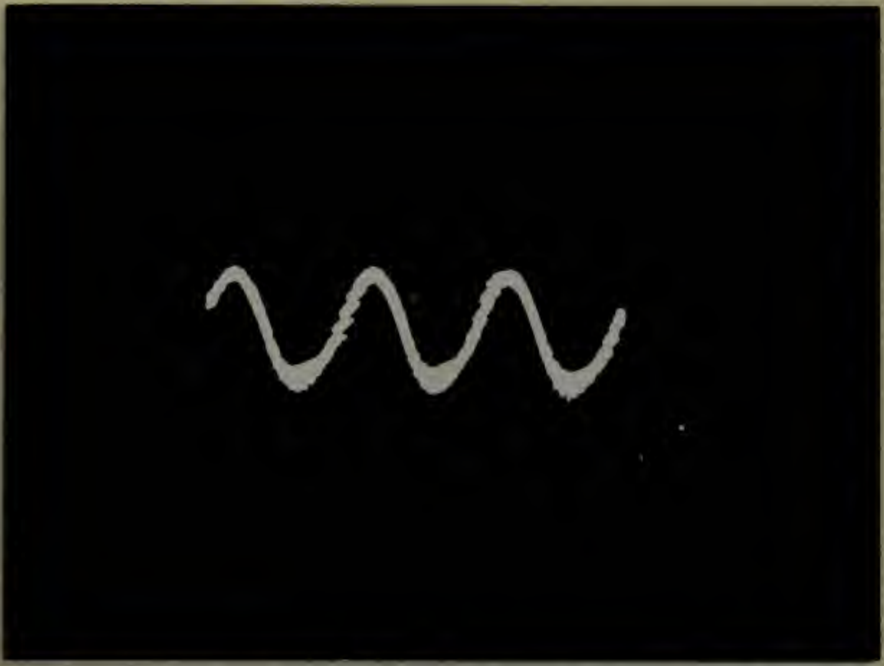


Fig. 4-1 (a) Output waveform with the pulse repetition frequency = 1000 pps.

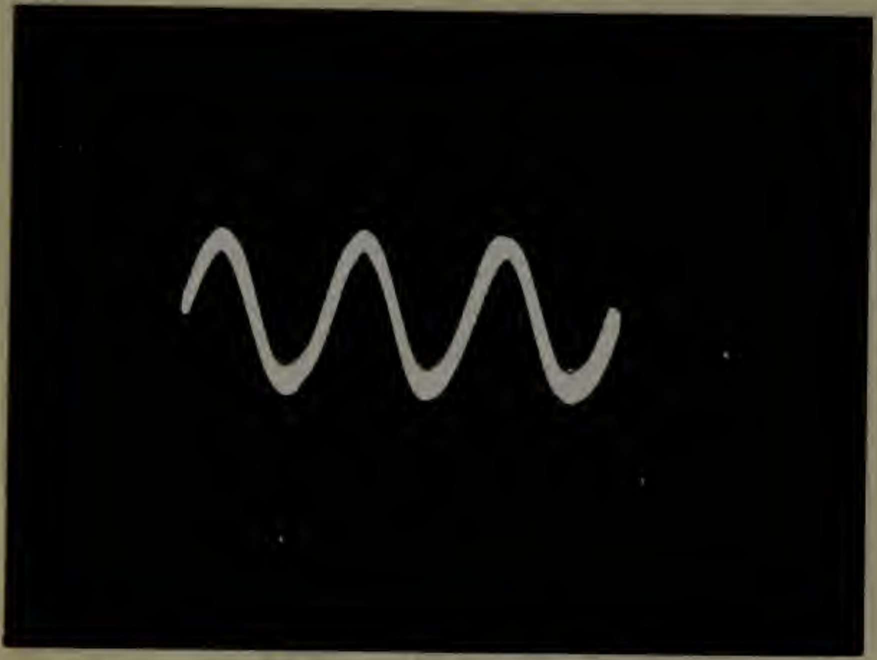


Fig. 4-1 (b) Output waveform with the pulse repetition frequency = 2000 pps.

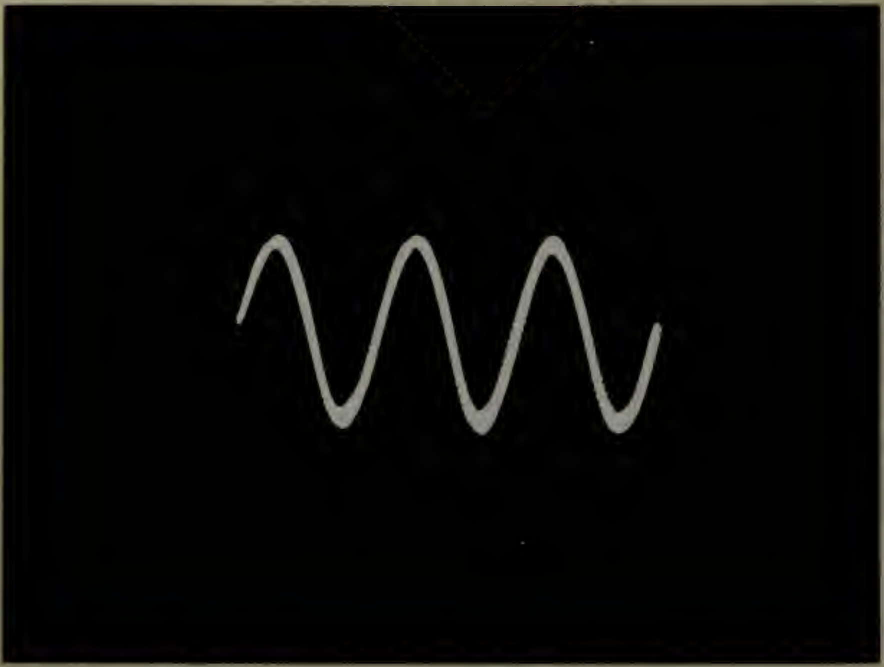


Fig. 4-1 (c) Output waveform with the pulse repetition frequency = 3000 pps.

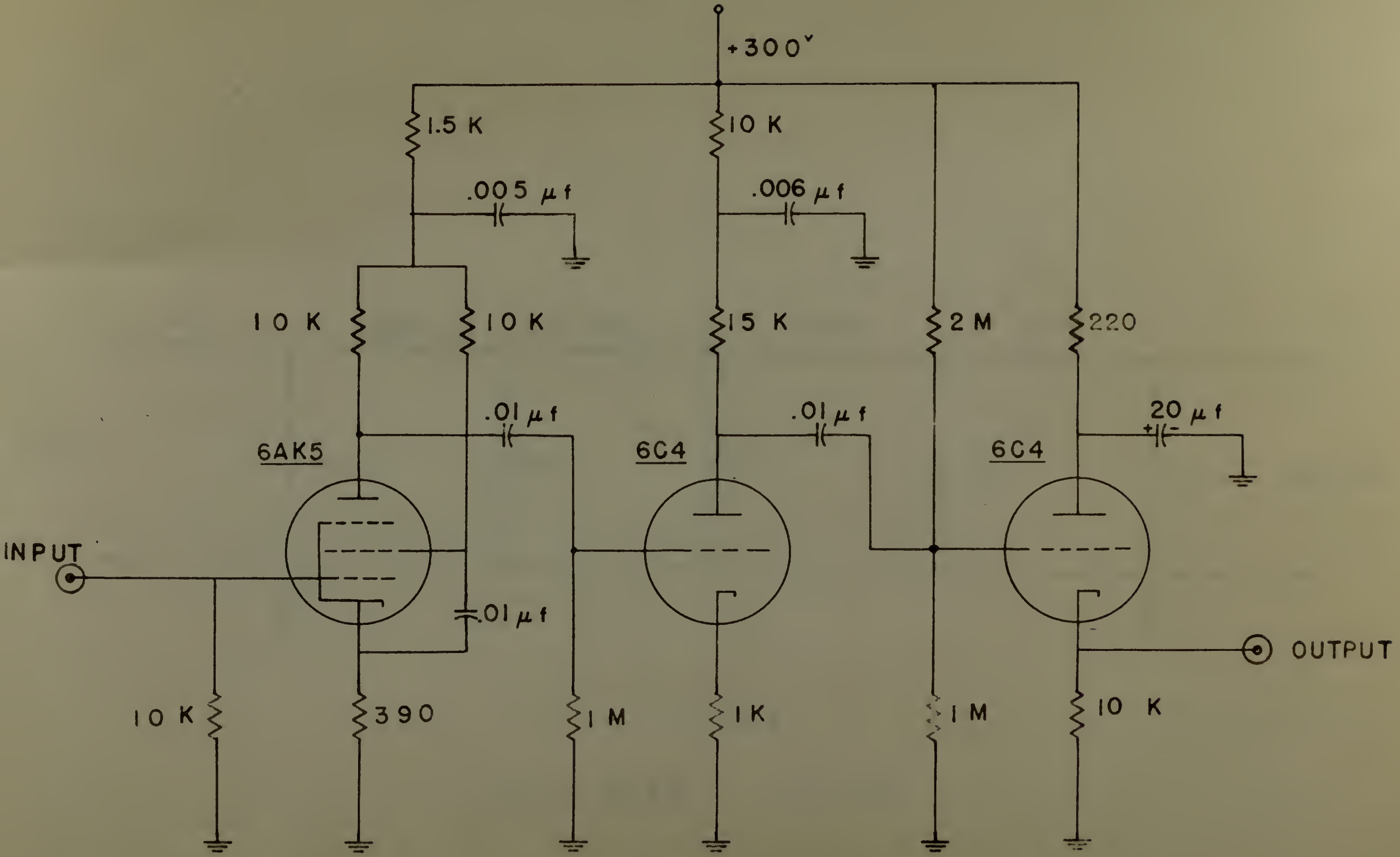


FIG. 4-2

PULSE AMPLIFIER

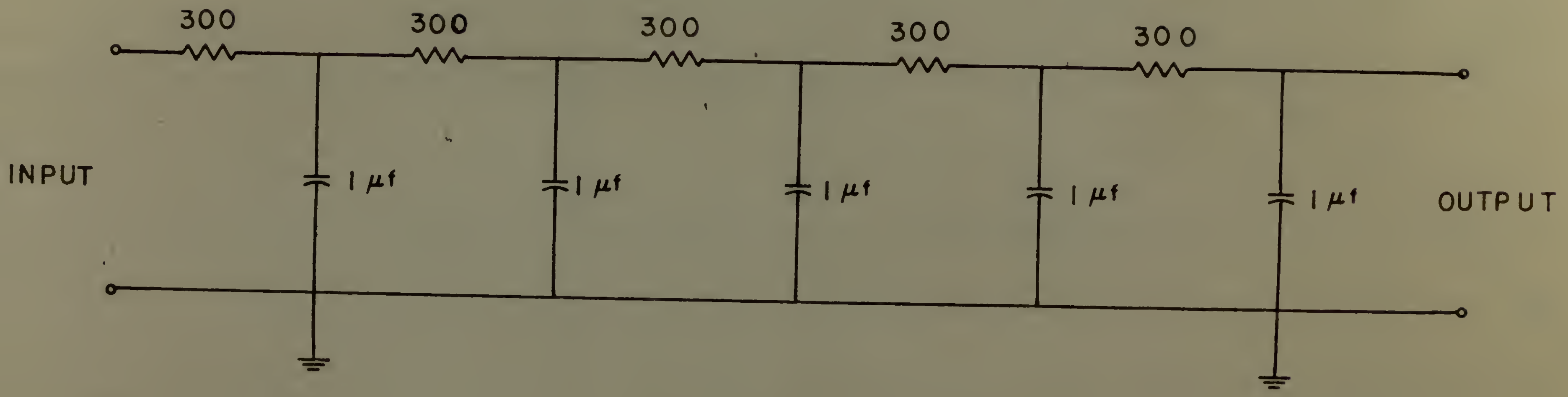
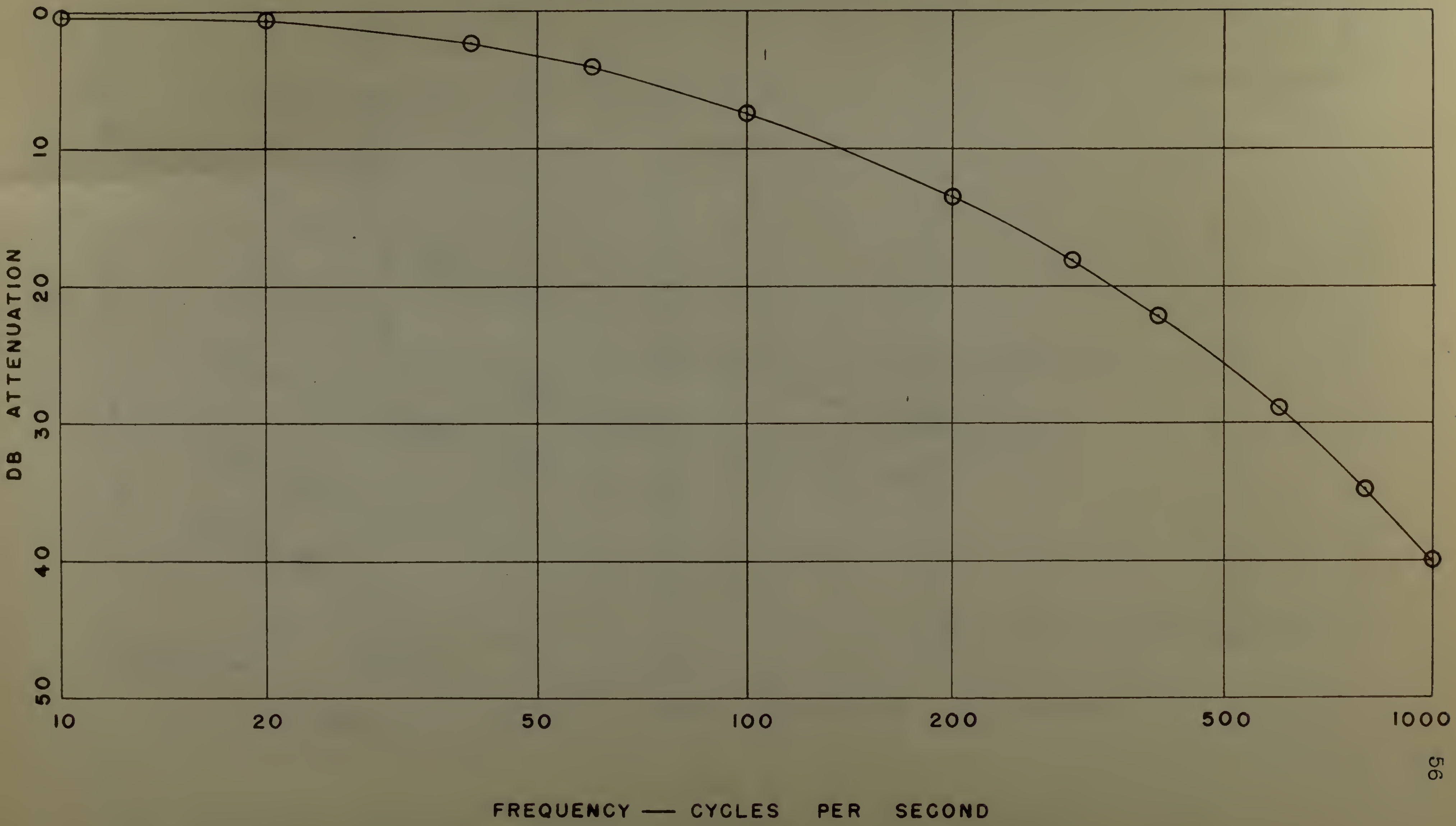


FIG. 4–3

LOW - PASS FILTER

FIG. 4-4

FILTER ATTENUATION VS. FREQUENCY



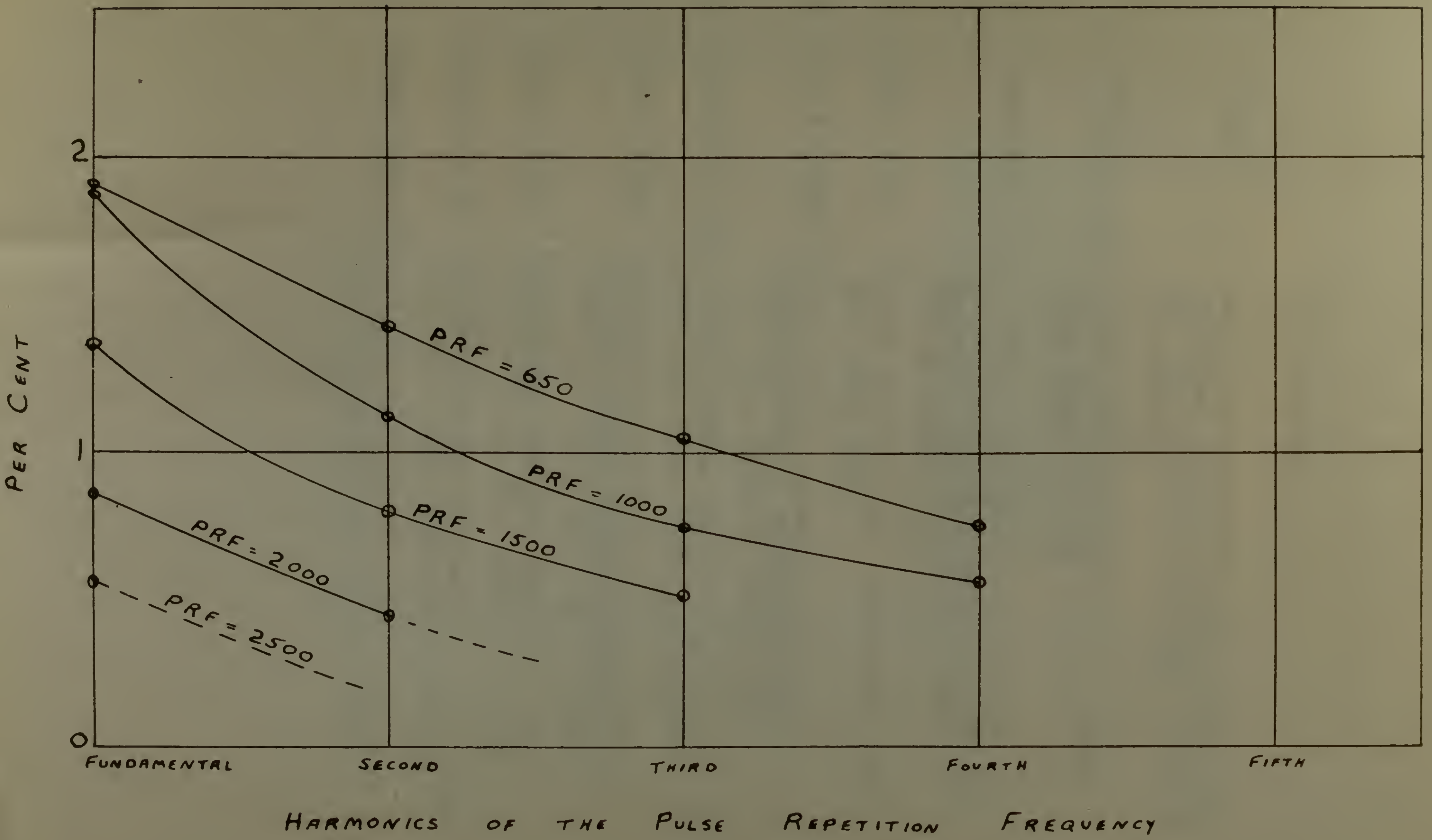


Fig. 4-5

Pulse Repetition Frequency Harmonics Appearing in the Output

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